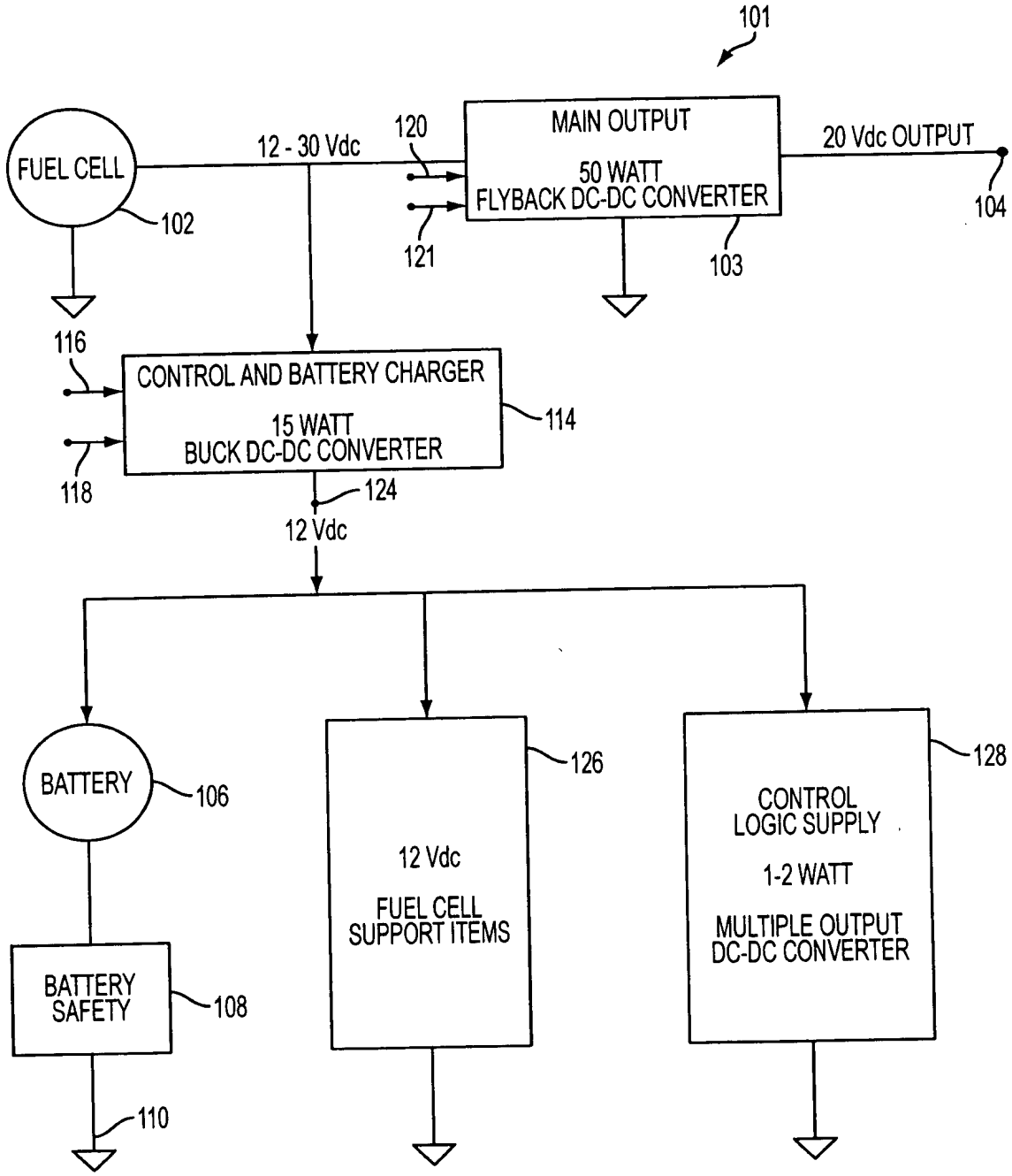

FIG. 1

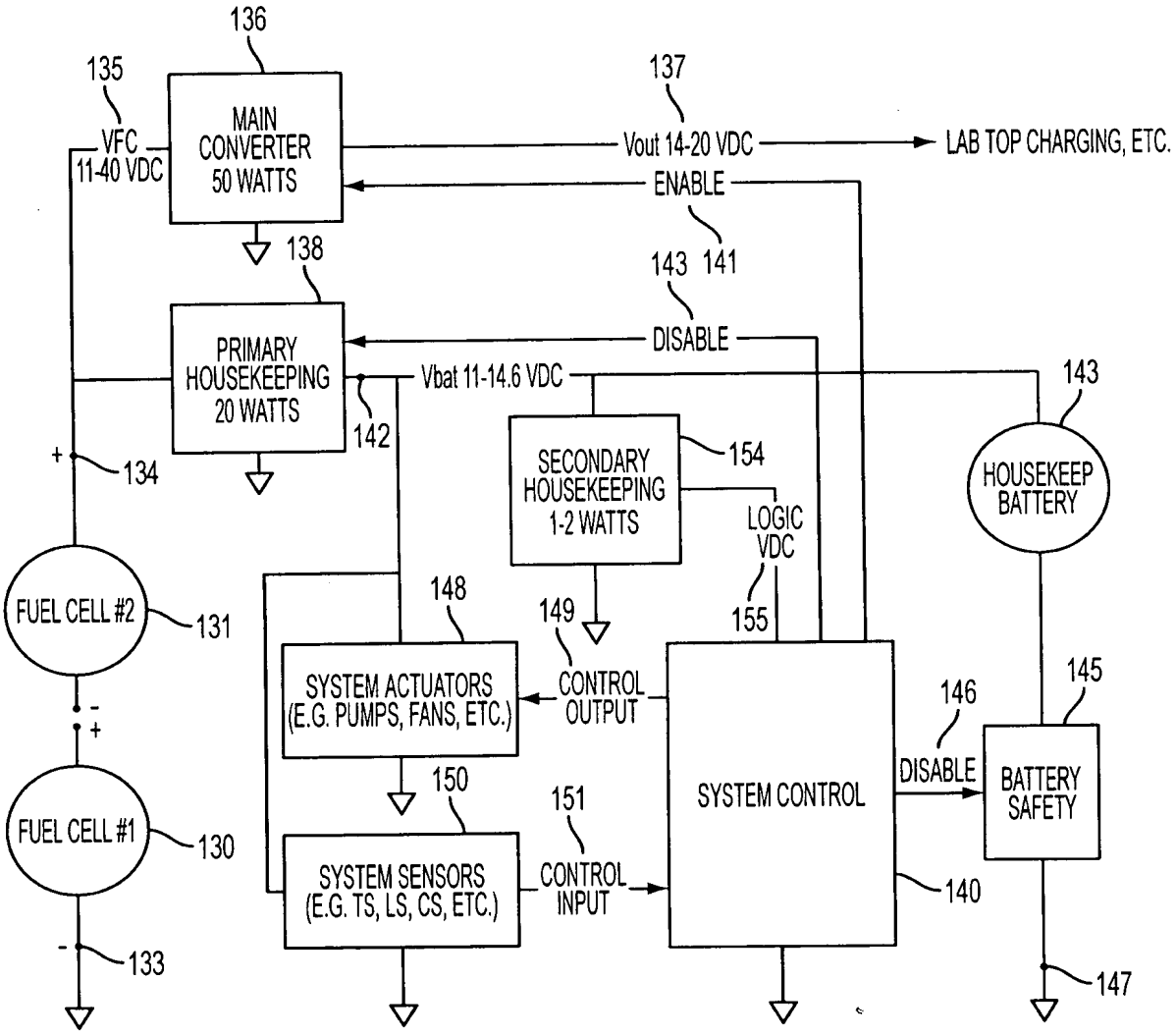
136
135
137
MAIN CONVERTER 50 WATTS
VFC 11-40 VDC
Vout 14-20 VDC
LAB TOP CHARGING, ETC.
ENABLE
138
143
141
DISABLE
PRIMARY HOUSEKEEPING 20 WATTS
Vbat 11-14.6 VDC
142
143
SECONDARY HOUSEKEEPING 1-2 WATTS
154
HOUSEKEEP BATTERY
LOGIC VDC
134
FUEL CELL #2
131
148
149
155
SYSTEM ACTUATORS (E.G. PUMPS, FANS, ETC.)
CONTROL OUTPUT
145
146
150
151
SYSTEM CONTROL
DISABLE
BATTERY SAFETY
FUEL CELL #1
130
SYSTEM SENSORS (E.G. TS, LS, CS, ETC.)
CONTROL INPUT
140
133
147

FIG. 2

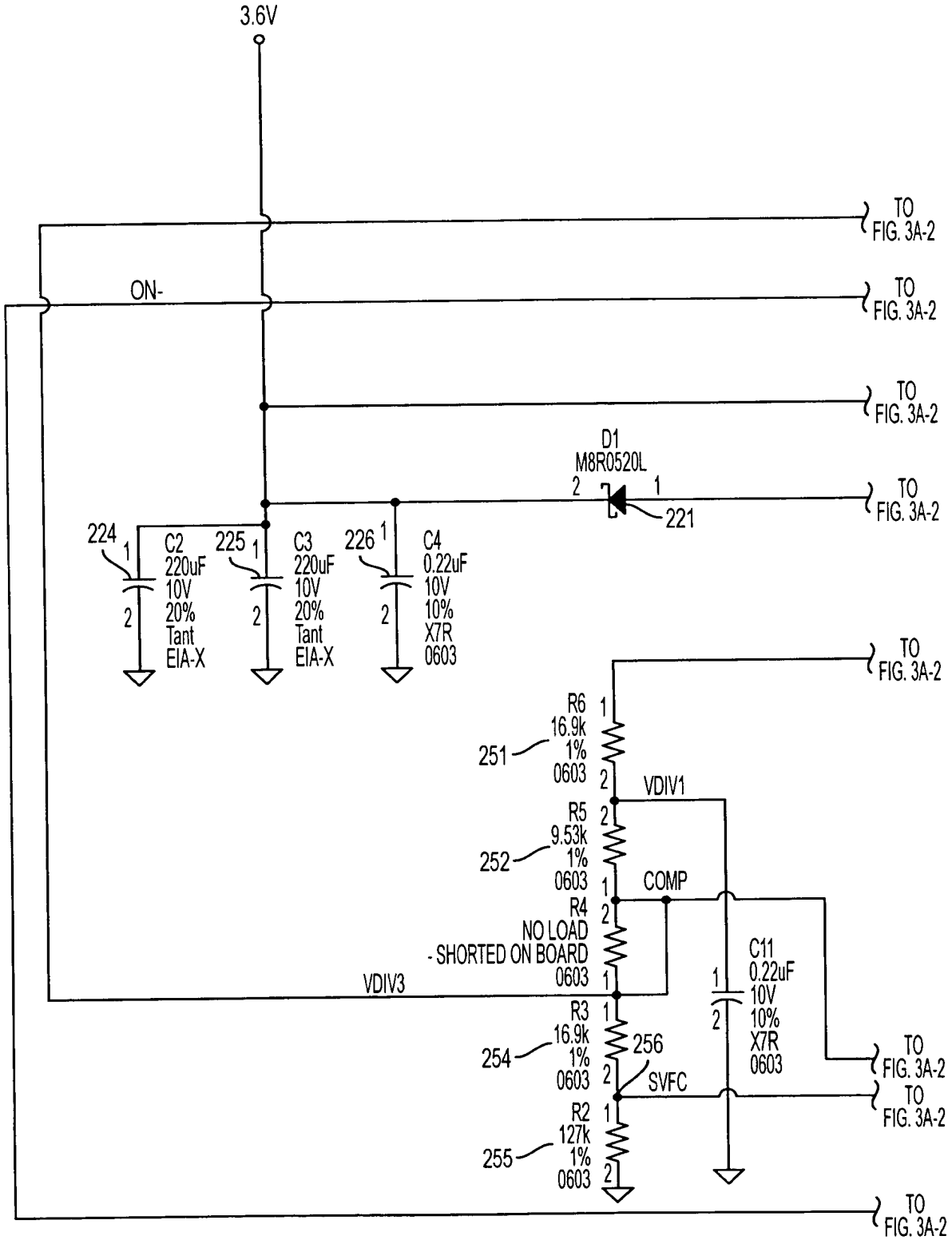
3.6V
ON-
TO FIG. 3A-2
TO FIG. 3A-2
TO FIG. 3A-2
D1
M8R0520L
TO FIG. 3A-2
221
224
C2
220uF
10V
20%
Tant
EIA-X
225
C3
220uF
10V
20%
Tant
EIA-X
226
C4
0.22uF
10V
10%
X7R
0603
TO FIG. 3A-2
R6
16.9k
1%
0603
251
VDIV1
R5
9.53k
1%
0603
252
COMP
R4
NO LOAD
- SHORTED ON BOARD
0603
VDIV3
C11
0.22uF
10V
10%
X7R
0603
R3
16.9k
1%
0603
254
256
SVFC
TO FIG. 3A-2
TO FIG. 3A-2
R2
127k
1%
0603
255
TO FIG. 3A-2

FIG. 3A-1

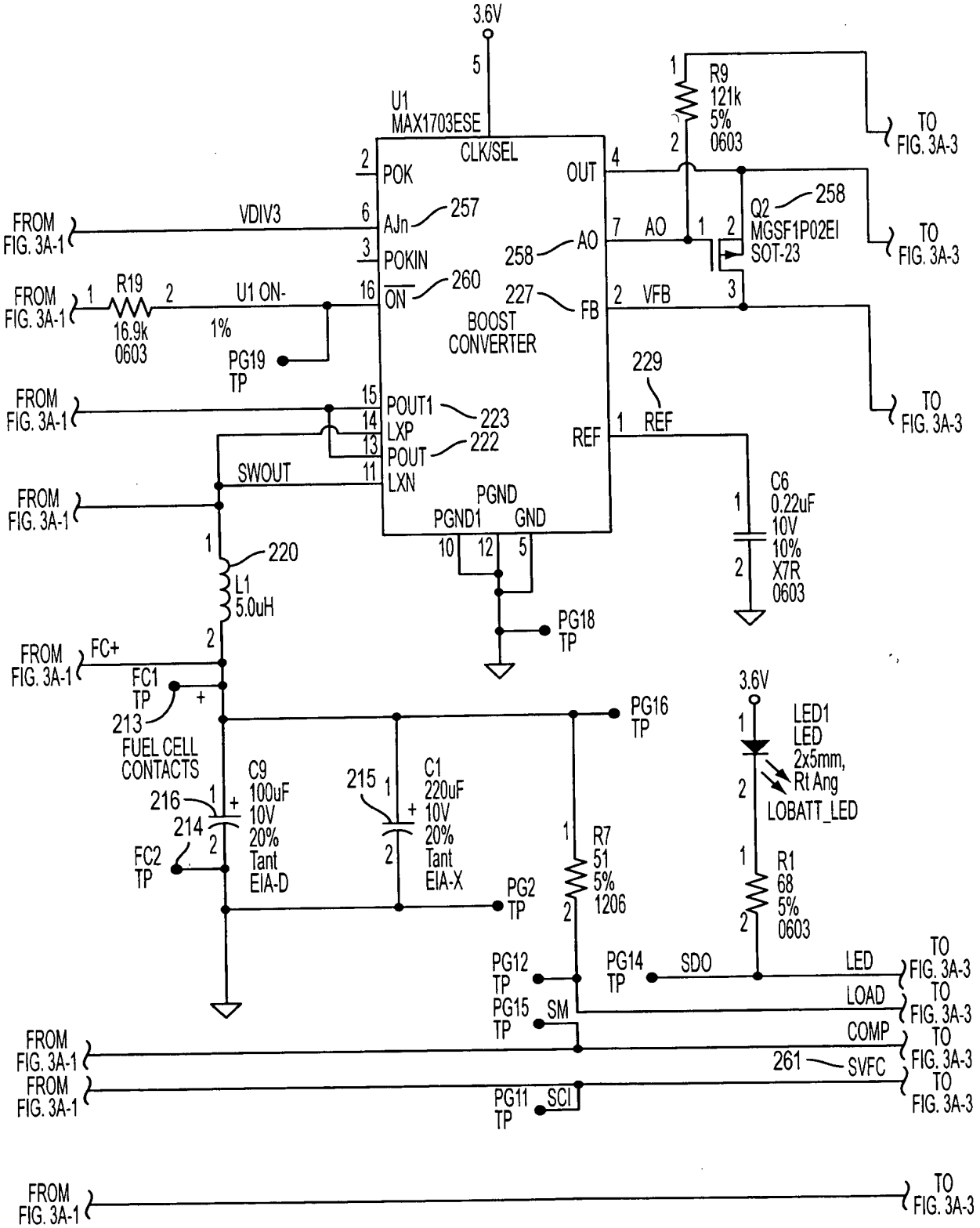
3.6V
U1
MAX1703ESE
CLK/SEL
POK
OUT
AJn
257
POKIN
AO
258
ON
260
FB
227
BOOST
CONVERTER
POUT1
223
LXP
POUT
222
LXN
REF
229
PGND
PGND1
GND
SWOUT
R9
121k
5%
0603
TO
FIG. 3A-3
Q2
258
MGSF1P02EI
SOT-23
VFB
FROM
FIG. 3A-1
VDIV3
R19
16.9k
0603
1%
U1 ON-
PG19
TP
C6
0.22uF
10V
10%
X7R
0603
220
L1
5.0uH
PG18
TP
FC+
FC1
TP
213
FUEL CELL
CONTACTS
PG16
TP
C9
100uF
10V
20%
Tant
EIA-D
216
214
FC2
TP
215
C1
220uF
10V
20%
Tant
EIA-X
PG2
TP
R7
51
5%
1206
LED1
LED
2x5mm,
Rt Ang
LOBATT_LED
R1
68
5%
0603
PG12
TP
PG14
TP
SDO
LED
LOAD
PG15
TP
SM
COMP
261
SVFC
PG11
TP
SCL

FIG. 3A-2

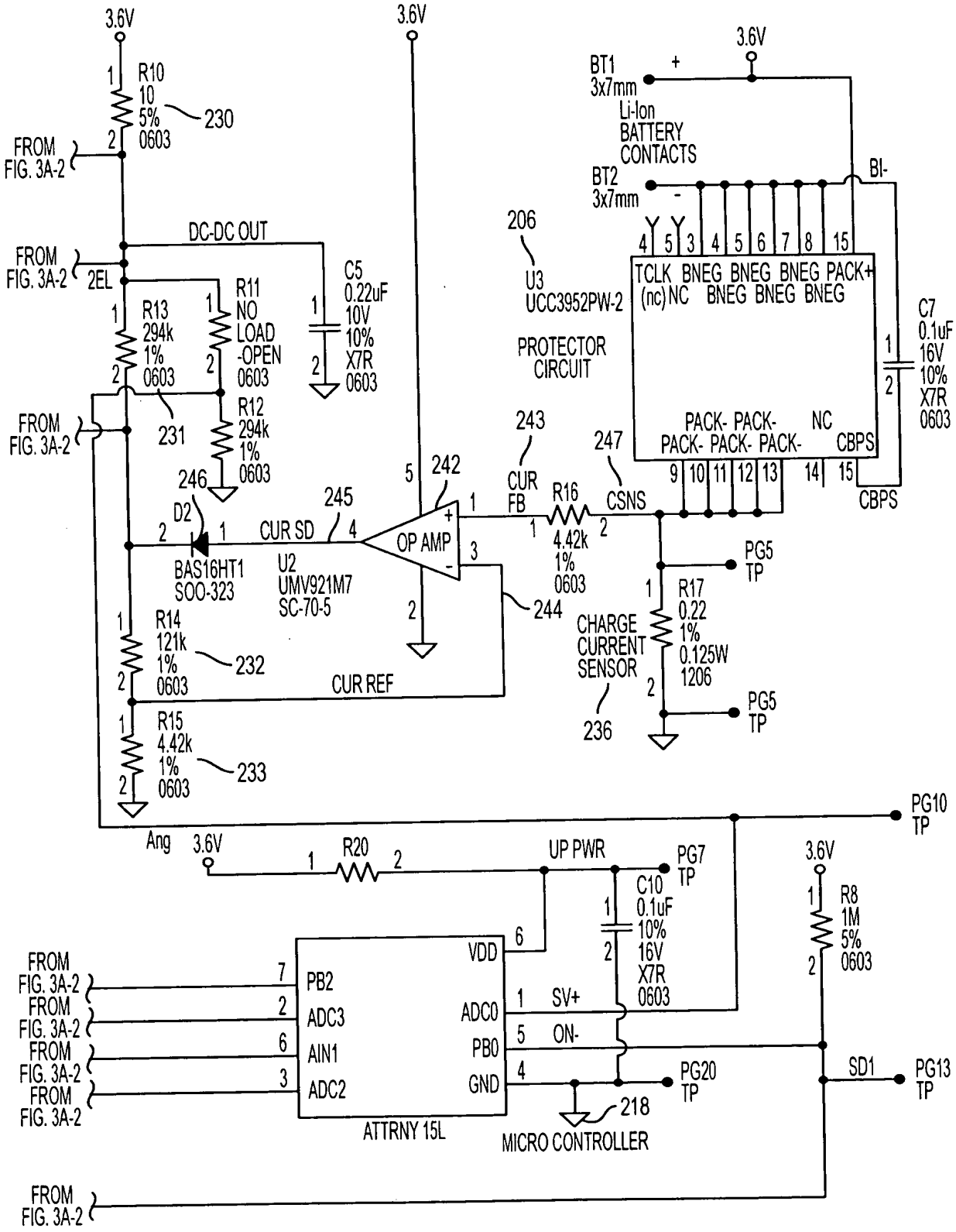
3.6V
R10
10
5%
0603
230
FROM FIG. 3A-2
DC-DC OUT
FROM FIG. 3A-2
2EL
R13
294k
1%
0603
R11
NO LOAD
-OPEN
0603
C5
0.22uF
10V
10%
X7R
0603
231
R12
294k
1%
0603
246
D2
BAS16HT1
SOO-323
CUR SD
245
U2
UMV921M7
SC-70-5
OP AMP
242
5
1
2
3
4
CUR FB
243
R16
4.42k
1%
0603
CSNS
247
244
R14
121k
1%
0603
232
CUR REF
R15
4.42k
1%
0603
233
BT1
3x7mm
Li-Ion
BATTERY
CONTACTS
BT2
3x7mm
BI-
206
U3
UCC3952PW-2
PROTECTOR
CIRCUIT
TCLK BNEG BNEG BNEG PACK+
(nc) NC BNEG BNEG BNEG
PACK- PACK- NC
PACK- PACK- PACK- CBPS
CBPS
C7
0.1uF
16V
10%
X7R
0603
PG5
TP
R17
0.22
1%
0.125W
1206
CHARGE
CURRENT
SENSOR
236
PG5
TP
PG10
TP
Ang
3.6V
R20
UP PWR
PG7
TP
C10
0.1uF
10%
16V
X7R
0603
R8
1M
5%
0603
FROM FIG. 3A-2
PB2
ADC3
AIN1
ADC2
VDD
ADC0
PB0
GND
SV+
ON-
ATTRNY 15L
PG20
TP
218
MICRO CONTROLLER
SD1
PG13
TP
FROM FIG. 3A-2

FIG. 3A-3

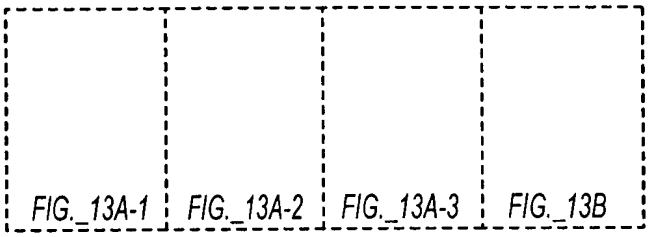
FIG._13A-1
FIG._13A-2
FIG._13A-3
FIG._13B

FIG. 3A

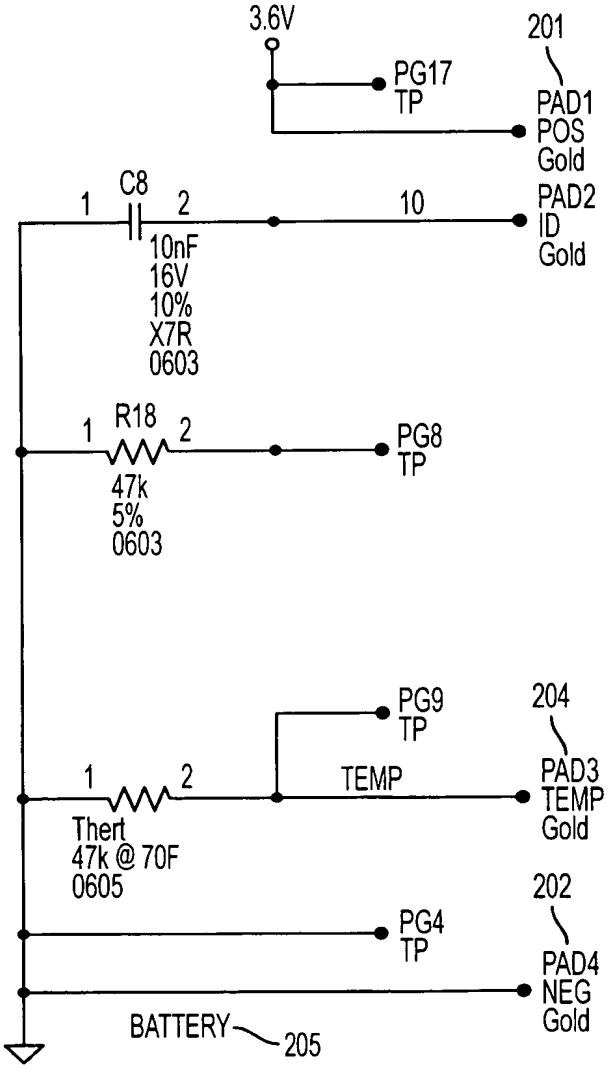
3.6V
201
PG17
TP
PAD1
POS
Gold
C8
1
2
10
PAD2
ID
Gold
10nF
16V
10%
X7R
0603
R18
1
2
PG8
TP
47k
5%
0603
PG9
TP
204
1
2
TEMP
PAD3
TEMP
Gold
Thert
47k @ 70F
0605
202
PG4
TP
PAD4
NEG
Gold
BATTERY
205

FIG. 3B

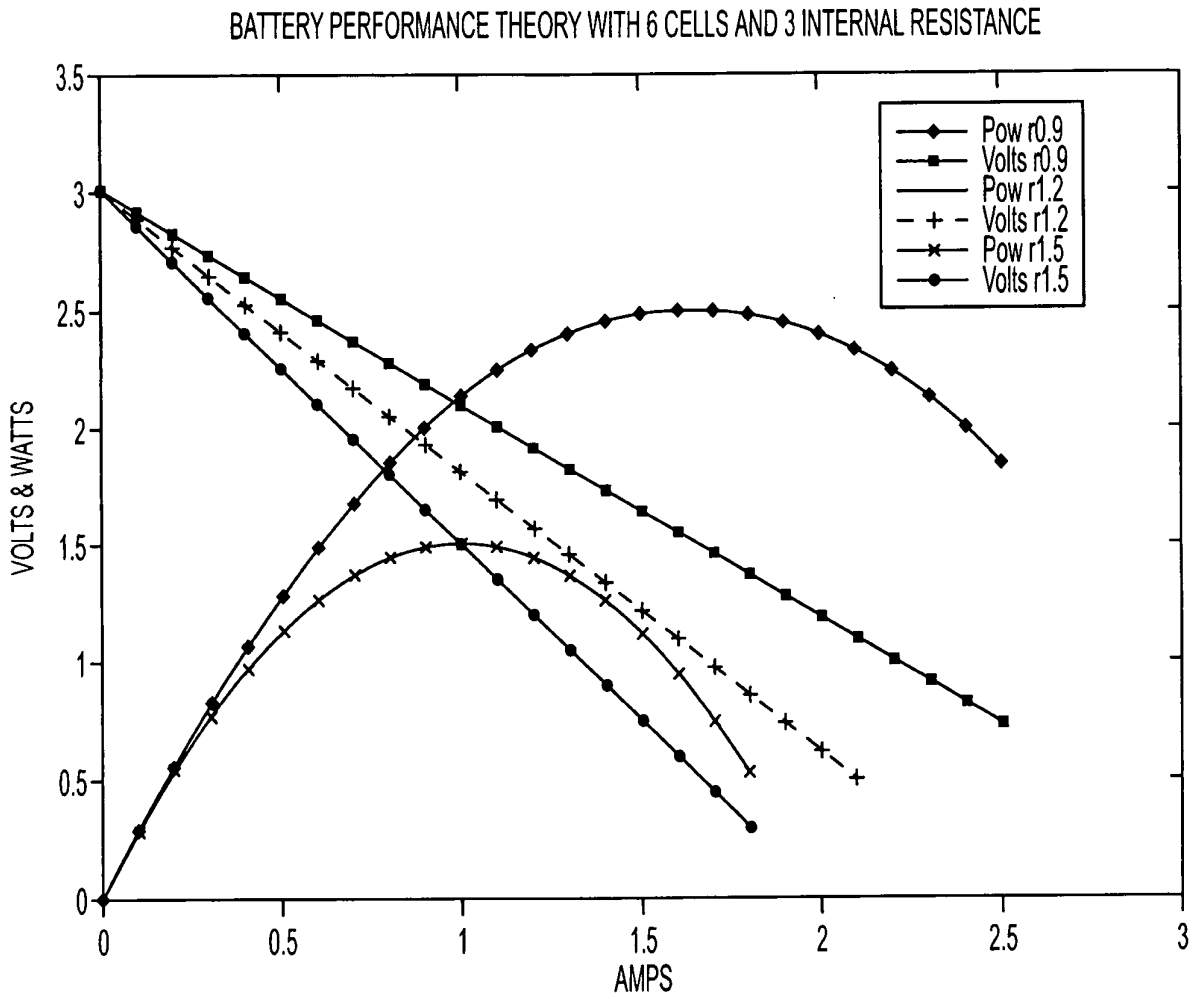
BATTERY PERFORMANCE THEORY WITH 6 CELLS AND 3 INTERNAL RESISTANCE
VOLTS & WATTS
AMPS
0
0.5
1
1.5
2
2.5
3
3.5
Pow r0.9
Volts r0.9
Pow r1.2
Volts r1.2
Pow r1.5
Volts r1.5

FIG. 4

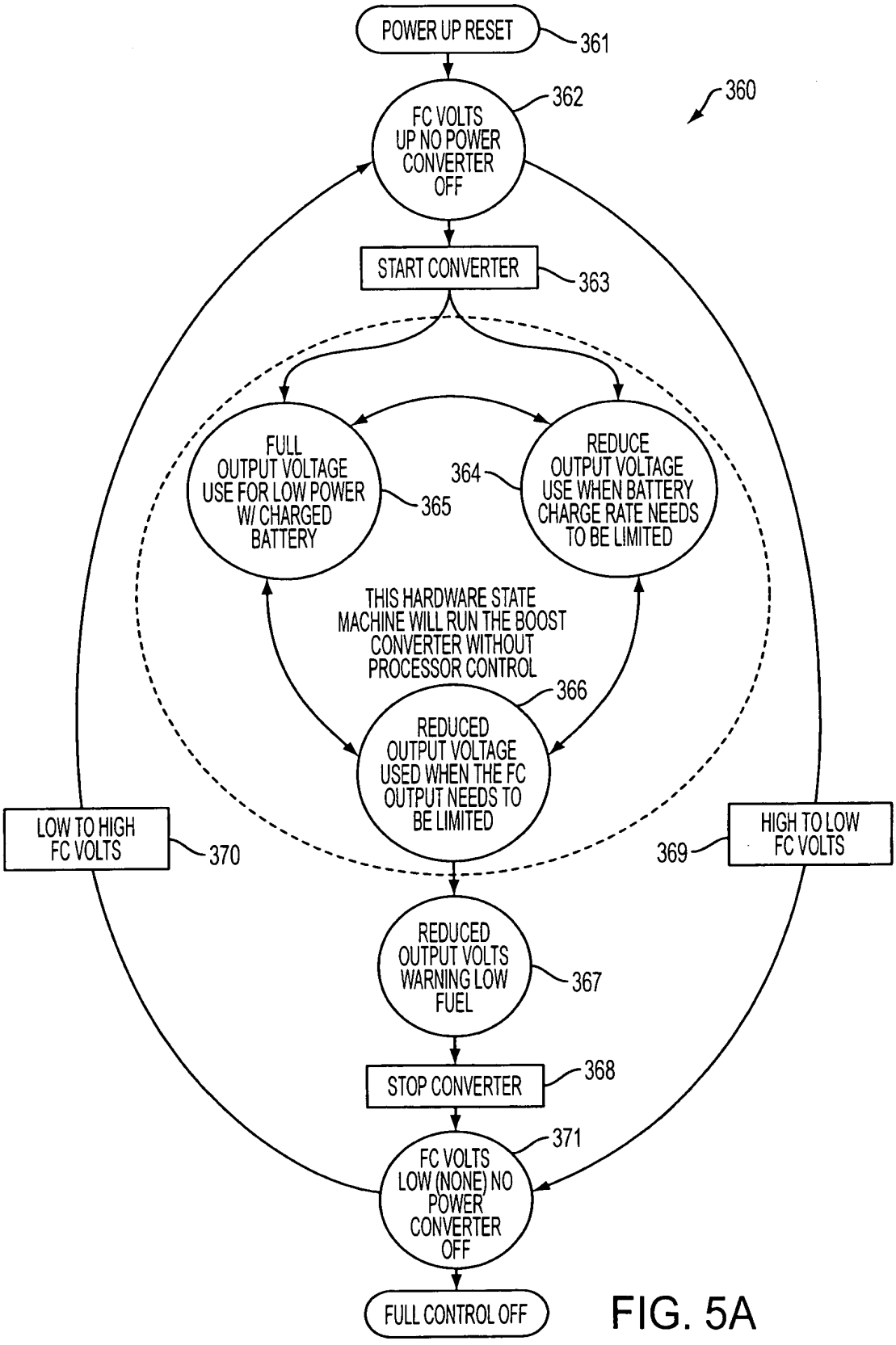
POWER UP RESET
361
360
FC VOLTS UP NO POWER CONVERTER OFF
362
START CONVERTER
363
FULL OUTPUT VOLTAGE USE FOR LOW POWER W/ CHARGED BATTERY
365
364
REDUCE OUTPUT VOLTAGE USE WHEN BATTERY CHARGE RATE NEEDS TO BE LIMITED
THIS HARDWARE STATE MACHINE WILL RUN THE BOOST CONVERTER WITHOUT PROCESSOR CONTROL
366
REDUCED OUTPUT VOLTAGE USED WHEN THE FC OUTPUT NEEDS TO BE LIMITED
LOW TO HIGH FC VOLTS
370
HIGH TO LOW FC VOLTS
369
REDUCED OUTPUT VOLTS WARNING LOW FUEL
367
STOP CONVERTER
368
371
FC VOLTS LOW (NONE) NO POWER CONVERTER OFF
FULL CONTROL OFF

FIG. 5A

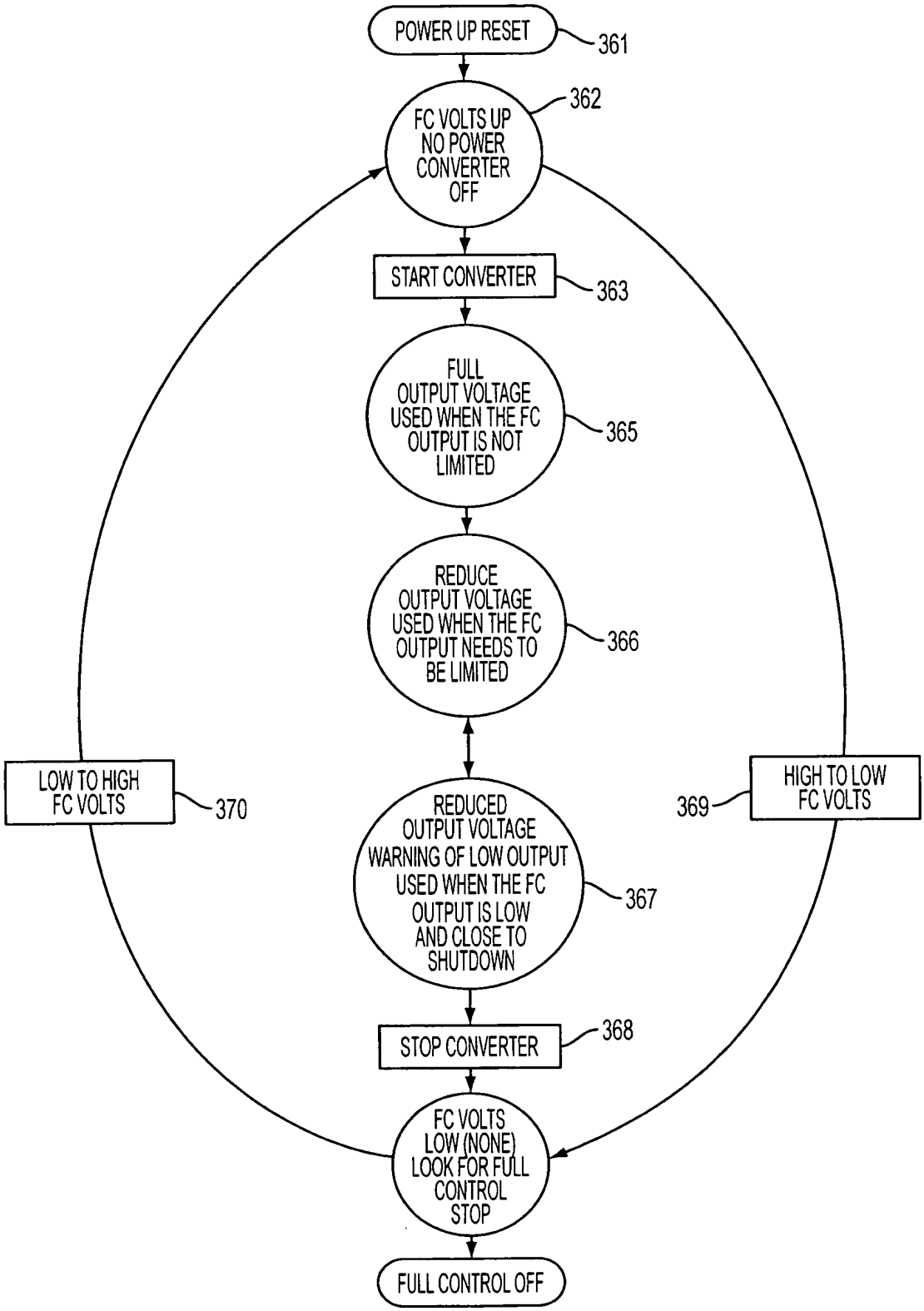
POWER UP RESET
361
FC VOLTS UP
NO POWER
CONVERTER
OFF
362
START CONVERTER
363
FULL
OUTPUT VOLTAGE
USED WHEN THE FC
OUTPUT IS NOT
LIMITED
365
REDUCE
OUTPUT VOLTAGE
USED WHEN THE FC
OUTPUT NEEDS TO
BE LIMITED
366
LOW TO HIGH
FC VOLTS
370
REDUCED
OUTPUT VOLTAGE
WARNING OF LOW OUTPUT
USED WHEN THE FC
OUTPUT IS LOW
AND CLOSE TO
SHUTDOWN
367
HIGH TO LOW
FC VOLTS
369
STOP CONVERTER
368
FC VOLTS
LOW (NONE)
LOOK FOR FULL
CONTROL
STOP
FULL CONTROL OFF

FIG. 5B

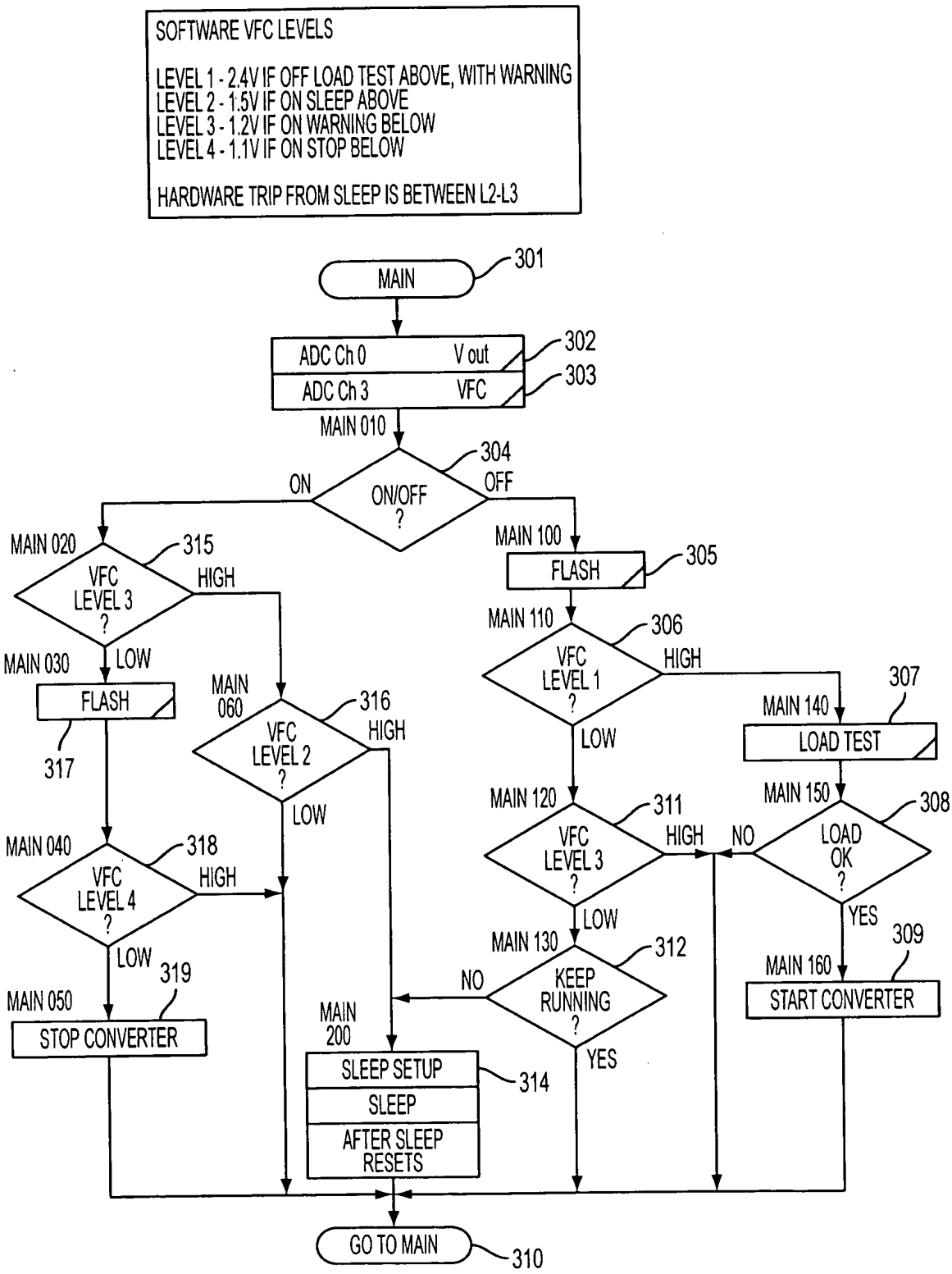
SOFTWARE VFC LEVELS
LEVEL 1 - 2.4V IF OFF LOAD TEST ABOVE, WITH WARNING
LEVEL 2 - 1.5V IF ON SLEEP ABOVE
LEVEL 3 - 1.2V IF ON WARNING BELOW
LEVEL 4 - 1.1V IF ON STOP BELOW
HARDWARE TRIP FROM SLEEP IS BETWEEN L2-L3
MAIN
301
ADC Ch 0
V out
302
ADC Ch 3
VFC
303
MAIN 010
ON/OFF ?
304
ON
OFF
MAIN 020
VFC LEVEL 3 ?
315
HIGH
LOW
MAIN 030
FLASH
317
MAIN 040
VFC LEVEL 4 ?
318
HIGH
LOW
MAIN 050
STOP CONVERTER
319
MAIN 060
VFC LEVEL 2 ?
316
HIGH
LOW
MAIN 100
FLASH
305
MAIN 110
VFC LEVEL 1 ?
306
HIGH
LOW
MAIN 120
VFC LEVEL 3 ?
311
HIGH
LOW
MAIN 130
KEEP RUNNING ?
312
NO
YES
MAIN 140
LOAD TEST
307
MAIN 150
LOAD OK ?
308
NO
YES
MAIN 160
START CONVERTER
309
MAIN 200
SLEEP SETUP
SLEEP
AFTER SLEEP RESETS
314
GO TO MAIN
310

FIG. 6

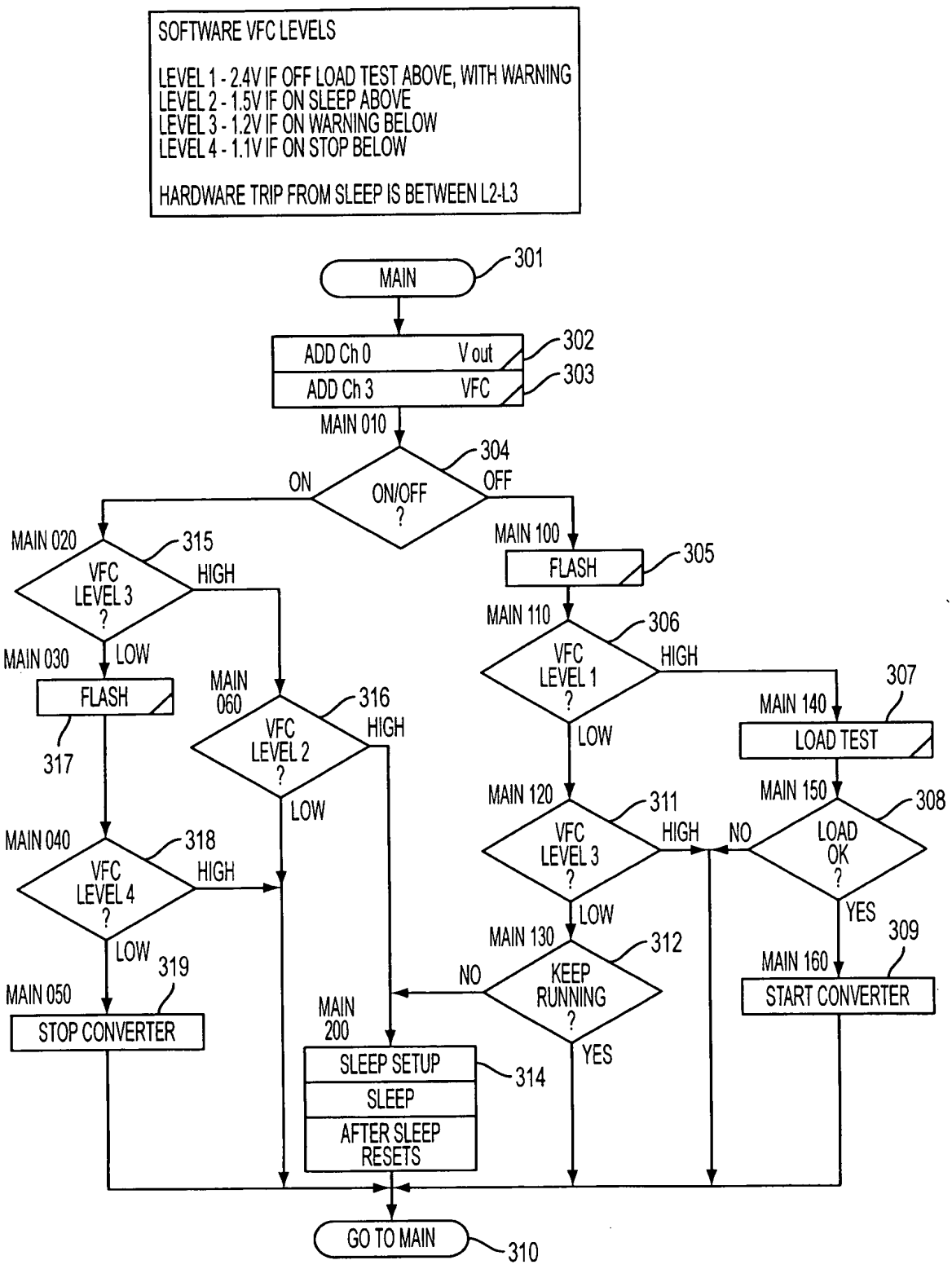
SOFTWARE VFC LEVELS
LEVEL 1 - 2.4V IF OFF LOAD TEST ABOVE, WITH WARNING
LEVEL 2 - 1.5V IF ON SLEEP ABOVE
LEVEL 3 - 1.2V IF ON WARNING BELOW
LEVEL 4 - 1.1V IF ON STOP BELOW
HARDWARE TRIP FROM SLEEP IS BETWEEN L2-L3
MAIN
301
ADD Ch 0
V out
302
ADD Ch 3
VFC
303
MAIN 010
ON/OFF ?
304
ON
OFF
MAIN 020
VFC LEVEL 3 ?
315
HIGH
LOW
MAIN 030
FLASH
317
MAIN 060
VFC LEVEL 2 ?
316
HIGH
LOW
MAIN 040
VFC LEVEL 4 ?
318
HIGH
LOW
MAIN 050
STOP CONVERTER
319
MAIN 100
FLASH
305
MAIN 110
VFC LEVEL 1 ?
306
HIGH
LOW
MAIN 120
VFC LEVEL 3 ?
311
HIGH
LOW
MAIN 130
KEEP RUNNING ?
312
NO
YES
MAIN 140
LOAD TEST
307
MAIN 150
LOAD OK ?
308
NO
YES
MAIN 160
START CONVERTER
309
MAIN 200
SLEEP SETUP
SLEEP
AFTER SLEEP RESETS
314
GO TO MAIN
310

FIG. 7A

```
; Code file for                    Stepup boost convertr
;
;
;
;
;
.include "tn15def.inc" ; supplies all std port and pin refances for tiny15
.include "constdef.inc" ; supplies init values
; regesters Defenations

.DEF    LOADOK      = r14    ; flag for load ok = 1
.DEF    TEMPF       = r15    ; Temp for flages
.DEF    VCCLOW      = r16    ; Voltage VCC
.DEF    VCCHIGH     = r17
.DEF    VFCLALOW    = r18    ; Voltage FC under load
.DEF    VFCLAHIGH   = r19
.DEF    VFCBALOW    = r20    ; Voltage FC main
.DEF    VFCBAHIGH   = r21
.DEF    VFCDIFLOW   = r23    ; Load difrance
.DEF    VFCDIFHIGH  = r24
.DEF    FLASHLOW    = r25    ; Flash Count for total stop
.DEF    FLASHHIGH   = r26
.DEF    TICB        = r27    ; tic count A
.DEF    TICA        = r28    ; tic count B
.DEF    TEMP        = r29    ; For I/O transfer
; Port B Pins definatiions
.EQU    ONNOT       = 0      ; Digital out port
.EQU    LED         = 2      ; Digital out port
.EQU    LOAD        = 4      ; Digital out port
.EQU    SVCC        = 0      ; ADC Channel
.EQU    SVFC        = 2      ; ADC Channel
.EQU    Comp        = 1      ; Port (Compartor)

.EQU    VCCLOWN     = 16     ; Reg pointer assignments
.EQU    VFCLAN      = 18     ; Reg pointer assignments
.EQU    VFCBAN      = 20     ; Reg pointer assignments

.EQU    FLASHDEL    = 50     ; 5 sec flash start delay
.EQU    TICFLASH    = 10     ; ticks per cycle
.EQU    LOADDEL     = 150    ; 15 sec to first load test
.EQU    TICLOAD     = 100    ; ticks per load test

.EQU    STOPED      = 1      ; flasher stioed

.CSEG
; TSR Vectors

        rjmp    RESET        ; Reset Handler
        reti    ;            External Intrupt, Not used
        reti    ;            Pin Change Handler, Not Used
        rjmp    TIM1_CMP     ; Timer 1 compare match, used for 0.1
sec tic

        reti;TIM1 OVF ;      Timer 1 overflow handler, Not used
        reti;TIM0_OVF ;      Timer 0 overflow handler, used for
short sub tic time

        reti;EE_RDY ;        EEPROM Ready handler
        reti;ANA_COMP ;      Analog Comparator Handler for Level
1.5 Fuel cell volts
```

FIG. 7B

```
                reti            ; ADC           ; ADC Conversion handler
MAIN:           ; Main Program start

                ; read adc Ch for SVcc base
                ldi             ZH, SVCC        ; set chanel
                ldi             ZL,VCCLOWN      ; data store pointer
                rcall           ADCRUN          ; call ACD Converter

                ; read adc ch for SVFC
                ldi             ZH, SVFC        ; set chanel
                ldi             ZL,VRCBAN       ; data store pointer
                rcall           ADCRUN          ; call ACD Converter
                ;ldi            VFCBAHIGH,$O3           ; • • • test for VFC
                ;ldi            VFCBALOW,$5e
                ;ldi            VFCLAHIGH,$02     ; • • • test for VFC
                ;ldi            VFCLALOW,$ff
                ;cbi            ddrB,onnot

MAIN010:        ; test OFF/ON
                sbic            PINB,ONNOT      ; read ON pin
                rjmp            MAIN100

MAIN020:        ; test vfc for level 3
                cpi             VFCBALOW,low(LEVEL3)
                ldi             TEMP,high(LEVEL3)
                cpc             VFCBAHIGH,TEMP
                brsh            MAIN060         ; the value is equ or high

MAIN030:        rcall           FLASH           ; do flash

MAIN040:        ; test vfc for level 4
                cpi             VFCBALOW,low(LEVEL4)
                ldi             TEMP,high(LEVEL4)
                cpc             VFCBAHIGH,TEMP
                brsh            MAIN            ; the value is equ or high, loop to

main            ; rjmp          MAIN050         ; the value is low fall or jump

MAIN050:        ; Stop the converter
                sbi             PORTB,ONNOT     ; Stop Converter and test led
                rjmp            MAIN            ; loop to main

MAIN060:        ; test vfc for level 2
                cpi             VFCBALOW,low(LEVEL2)
                ldi             Temp,high(LEVEL2)
                cpc             VFCBAHIGH, TEMP
                brsh            MAIN200         ; the value is equ or high
                rjmp            MAIN            ; the value is low fall or jump

                ; do flashe
MAIN100:        rcall           FLASH           ; do flash

MAIN110:        ; test vfc for level 1
                cpi             VFCBALOW,low(LEVEL1)
                ldi             TEMP,high(LEVEL1)
                cpc             VFCBAHIGH,TEMP
                brsh            MAIN140         ; the value is equ or high
                ; rjmp          MAIN120         ; the value is low fall or jump

MAIN120:        ; test vfc for level 3
                cpi     VFCBALOW, low(LEVEL3)
                ldi     TEMP,high(LEVEL3)
                cpc     VFCBAHIGH,TEMP
```

FIG. 7C

```
                brsh        MAIN            ; the value is equ or high
                ; rjmp      MAIN130         ; the value is low fall or jump
MAIN130:        ; test Flasher for stoped
                cpi         FLASHHIGH, STOPED
                breq        MAIN200         ; we need to sleep
                rjmp        MAIN            ; keep logging
MAIN140:        ; do load test
                rcall       LOADTEST        ; test the load
MAIN150:        ; Test for Load OK
                tst         LOADOK
                breq        MAIN            ; go to main
MAIN160:        ; start the converter
                cbi         PORTB, ONNOT    ; Start Converter
                clr         FLASHLOW        ; Stop Flashing
                clr         FLASHHIGH
                rjmp        MAIN            ; keep looping
MAIN200:        ; enter sleep mode
                cbi         ADCSR, ADEN     ; Power down the ADC
                clr         TICA
                clr         TICB
                ldi         TEMP, 0         ; stop timer int
                out         TIMSK, TEMP
                ldi         TEMP, MCUCRSET  ; set for idel
                out         MCUCR, TEMP
                ; may have to stop timers adc intrrupts
                ;sbi        ddrb, led       ;*******
                sleep       ; wate COMPARE
                ;cbi        ddrb, led       ; *****
MAIN210:        ; nop
                ; nop
                ; rjmp      MAIN210         ; we will wate to hear for a low level 2
transet
                ldi         TEMP, TIMSKSET  ; Enable timer int
                out         TIMSK, TEMP
                sbi         ADSCR, ADEN     ; Power up the ADC
                rjmp        MAIN            ; back to looping

; Place init code hear
RESET:          ; Clear Requesters
                clr         r0              ; Clear a master
                ldi         z1,29           ; Point to req r29
                st          z,r0            ; Clear
RESET01:        dec z1      ; set for next
                brne        RESET01         ; loop
                ; Setup the ADC
                ldi         TEMP, ADCSRSET
                out         ADCSR, TEMP
                sbi         ADCSR, ADEN     ; Power up the ADC
                ; Setup the comparitor
                ldi         TEMP, ACSRSET
                out         ACSR, TEMP
                ; Setup timer 0 for div 64
                ldi         TEMP, TCCR0SET
```

FIG. 7D

```
                        out     TCCR0, TEMP
                        ; Setup Timer 1 for 1.ms int
                        ldi     TRMP, TCCR1SET
                        out     TCCR1, TEMP
                        ldi     TEMP, OCR1ASET
                        out     OCR1A, TEMP
                        ; Setup Port B
                        ldi     TEMP, DDRBSET   ; Data direction
                        out     DDRB, TEMP
                        ldi     TEMP, PORTBSET
                        out     PORTB, TEMP
                        ; ldi   ticb, 100
                        ; Enable Interrupts
                        ldi     TEMP, TIMSKSET  ; Enable timer int
                        out     TIMSK, TEMP
                        ldi     TEMP, GIMSKSET  ; Set the mask
                        out     GIMSK, TEMP
                        ldi     TEMP, SREGSET   ; Enable
                        out     SREG, TEMP
                        ; Setup sleep
                        ldi     TEMP, MCUCRSET
                        out     MCUCR, TEMP
                        ; setup start delays
                        ldi     TICA, FLASHDEL  ; flash start delay
                        ldi     TICB, LOADDEL   ; load start delay
RESETEND:               rjmp    MAIN

; This ISR will dec the Time regesters tica and ticb to 0
TIM1_CMP:
                        in      TEMPF, SREG     ; save status
                        tst     tica
                        breq    tic01
                        dec     tica
Tic01:                  tst     ticb
                        breq    tic02
                        dec     ticb
Tic02:                  out     SREG, TEMPF     ; Restor status
                        reti

; This ISR will handal end of time 0 overflows
TIM0_OVF:               ; we ret at vector
                        reti

; This ISR will handal changes in FC Volts it will retern to last place
ANA_COMP:
                        ; we may whant to fix timer for fast service in main
                        reti

ADC:                    reti

EE_RDY                  reti                    ; This ISR may be used
later

TIM1_OVF:               reti                    ; This ISR will be
disabled
```

FIG. 7E

```
; Rutine to manage low fuel flasher
; The two byte flash count also acts as a run flag as follows:
;                   Low byte not 0, the counter is active and flashing
;                   Low byte equ 0, the high byte has meaning as follws:
;                                       0 =  clear to start flashing
;                                       1 =  flash time complet
;
;                                       any other go to sleep
FLASH:                                  ; Start Flasher
                                        tst     TICA            ; test for time to run
                                        brne    FLASHEND        ; must be zero th run
                                        ldi     TICA, TICFLASH  ; reset the timer

                                        tst     FLASHLOW        ; test for need
                                        brne    FLASH10         ; go to flashing
                                        tst     FLASHHIGH       ; test for stoped
                                        brne    FLASHEND        ; the flasher is stoped

                                        ; Start the flasher
                                        ldi     FLASHLOW, LOW(FLASHSET)
                                        ldi     FLASHHIGH, HIGH(FLASHSET)

FLASH10:                                ; flash the LED
                                        cbi     PORTB, LED      ; LED lamp on

                                        ; time the flash
                                        ldi     TEMP, TIME40m   ; load time value
                                        rcall   WATE            ; wate for time
                                        ;out    TCNT0, TEMP
                                        ;ldi    TEMP, MCUCRSET  ; set for idel
                                        ;out    MCUCR, TEMP
                                        ;sleep

                                        ; stop the flash
                                        sbj     PORTB, LED      ; LED lamp off

                                        ; count the flashes
                                        inc     FLASHLOW        ; Adjust Count
                                        brne    FLASHEND
                                        inc     FLASHLOW        ; Can not be zero
                                        inc     FLASHHIGH       ; Adjust high byte
                                        brne    FLASHEND
                                        clr     FLASHLOW        ; Flash time is over stop flash
                                        inc     FLASHHIGH       ; Set stoped
FLASHEND:                               ret

ADCRUN:                                 ; rutine for ADC
                                        ldi     TEMP, ADMUXSET
                                        add     TEMP, ZH
                                        out     ADMUX, TEMP     ; Set adc chanel
                                        sbi     ADCSR, ADSC     ; Start the ADC Conversion
                                        ;ldi    TEMP, MCUCRADC  ; set for ADC
                                        ;out    MCUCR, TEMP
                                        ;sleep                  ; wate for adc end
ADCRUN01:                               sbis    ADCSR, ADIF     ; Test for end of conversion
                                        rjmp    ADCRUN01        ; Loop till end
                                        in      TEMP, ADCL      ; Get the resulats
                                        st      Z, TEMP
                                        inc     ZL
                                        in      TEMP, ADCH      ; Get the resulats
                                        st      Z, TEMP
```

FIG. 7F

```
                ret
LOADTEST:       clr     LOADOK          ; make load not OK
                ; work load test
                tst     TICB            ; test for time to run
                brne    LOADTESTEND     ; must be zero th run
                ldi     TICB, TICLOAD   ; reset the timer
                sbi     DDRB, LOAD      ; start Load by seting output
                ; time the load
                ldi     TEMP, TIME20m   ; load timer to start
                rcall   WATE
                ;out    TCNT0, TEMP
                ;ldi    TEMP, MCUCRSET  ; set for idel
                ;out    MCUCR, TEMP
                ;sleep  ; wate for time
                ; read adc ch for SVFC
                ldi     ZH, SVFC        ; set chanel
                ldi     ZL, VFCLAN      ; data store pointer
                rcall   ADCRUN
                cbi     DDRB, LOAD      ; stop Load by try stating
                ; find load dif
                mov     VFCDIFLOW, VFCBALOW
                mov     VFCDIFHIGH, VFCBAHIGH
                sub     VFCDIFLOW, VFCLALOW
                sbc     VFCDIFHIGH, VFCLAGHIGH
                ; test dif
                cpi     VFCDIFLOW, low(loaddelta)
                ldi     TEMP, high(loaddelta)
                cpc     VFCDIFHIGH, TEMP
                brsh    LOADTESTEND
LOAD10:         doc     LOADOK          ; set load OK $FF
LOADTESTEND:    ret

; runtine to use timer 0 for wating, Temp  time
WATE:           ;
                out     TCNT0, TEMP
                ldi     TEMP, MCUCRSET  ; set for idel
                out     MCUCR, TEMP
                sleep   ; wate for time
                ret

Trace:          ; A lamp blinb rutine for testing
                sbic    PINb, led
                rjmp    Tracel
                sbi     PORTb, led
                cbi     PORTb, onnot
                rjmp    Traceend
Tracel:         cbi     PORTb, led
                sbi     PORTb, onnot
Traceend:       ret
EXIT
```

FIG. 7G

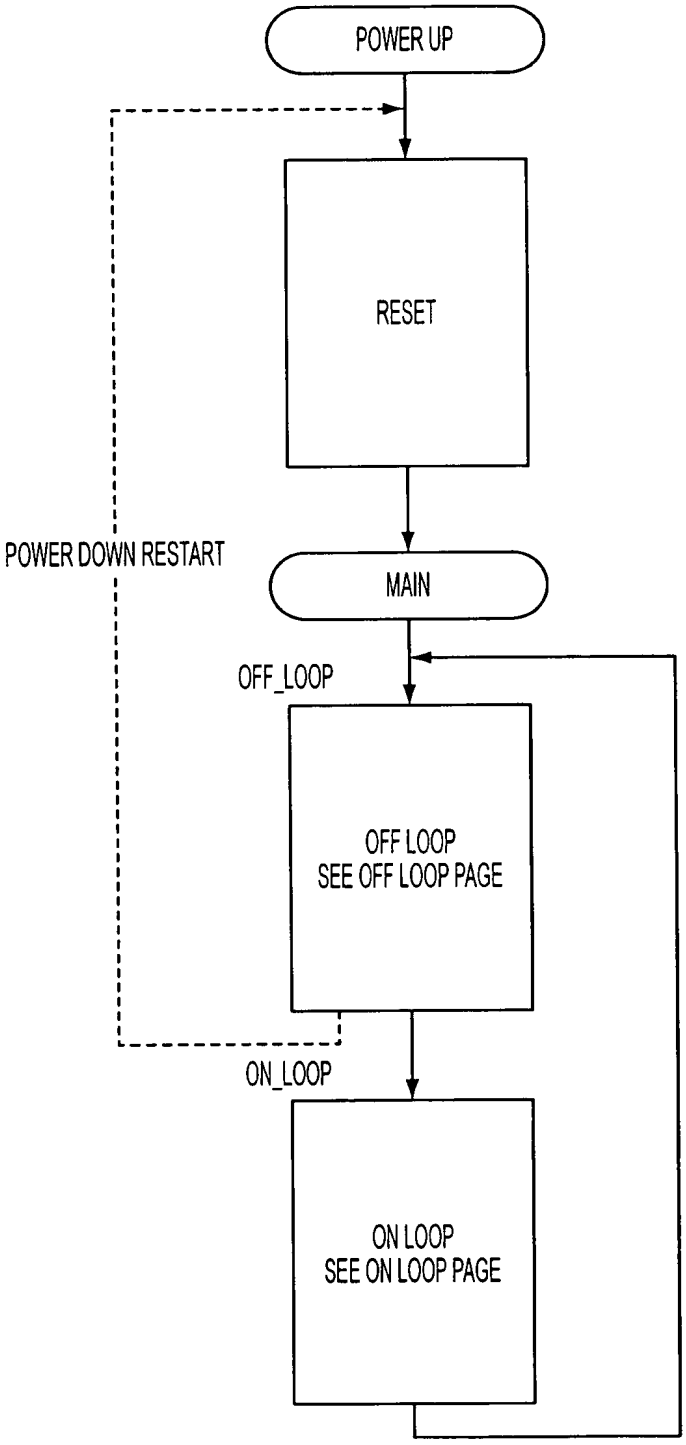
POWER UP
RESET
POWER DOWN RESTART
MAIN
OFF_LOOP
OFF LOOP
SEE OFF LOOP PAGE
ON_LOOP
ON LOOP
SEE ON LOOP PAGE

FIG. 8A

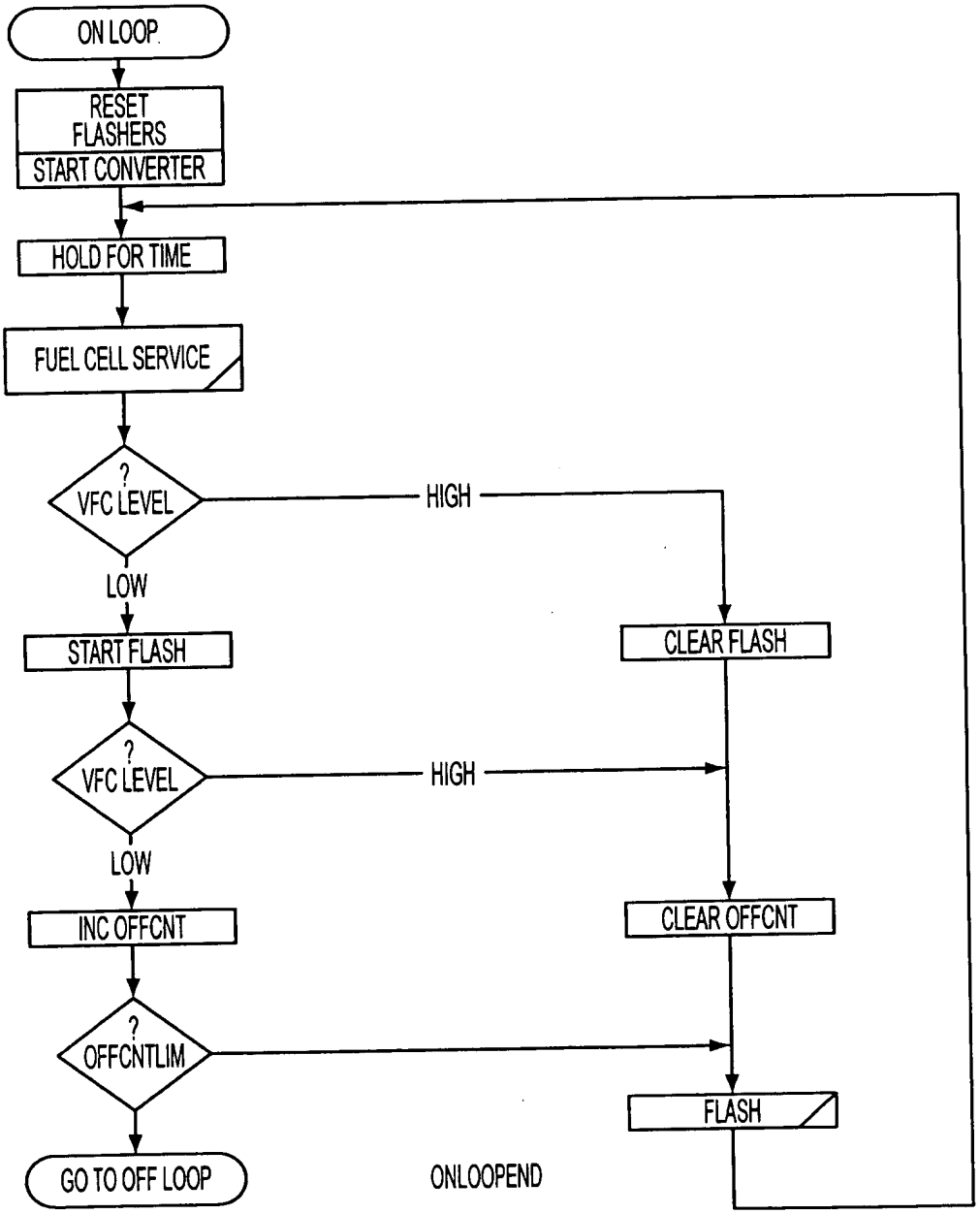
ON LOOP
RESET FLASHERS
START CONVERTER
HOLD FOR TIME
FUEL CELL SERVICE
? VFC LEVEL
HIGH
LOW
START FLASH
CLEAR FLASH
? VFC LEVEL
HIGH
LOW
INC OFFCNT
CLEAR OFFCNT
? OFFCNTLIM
FLASH
GO TO OFF LOOP
ONLOOPEND

FIG. 8B

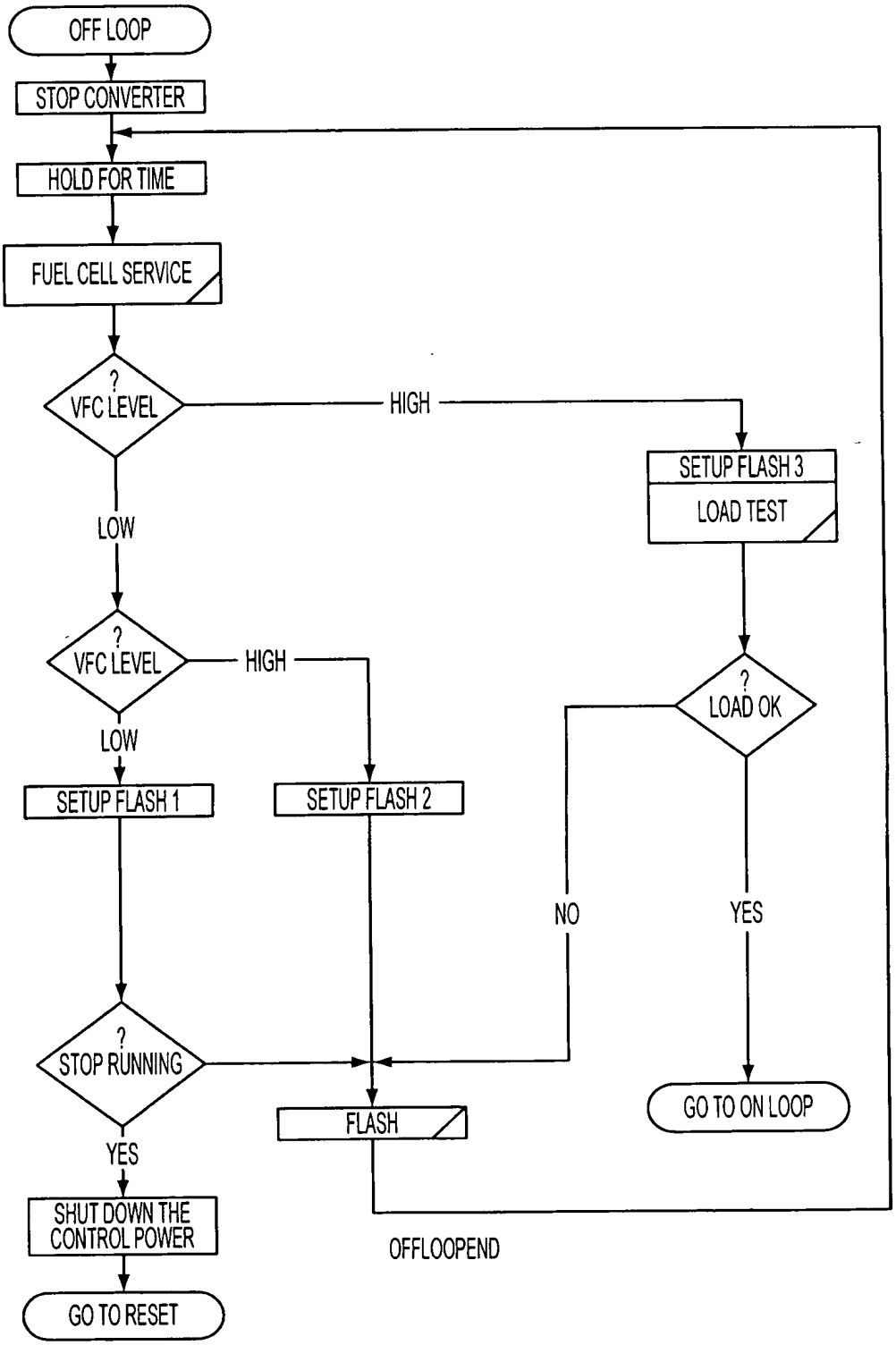
OFF LOOP
STOP CONVERTER
HOLD FOR TIME
FUEL CELL SERVICE
? VFC LEVEL
HIGH
LOW
SETUP FLASH 3
LOAD TEST
? VFC LEVEL
HIGH
LOW
? LOAD OK
SETUP FLASH 1
SETUP FLASH 2
NO
YES
? STOP RUNNING
FLASH
GO TO ON LOOP
YES
SHUT DOWN THE CONTROL POWER
OFFLOOPEND
GO TO RESET

FIG. 8C

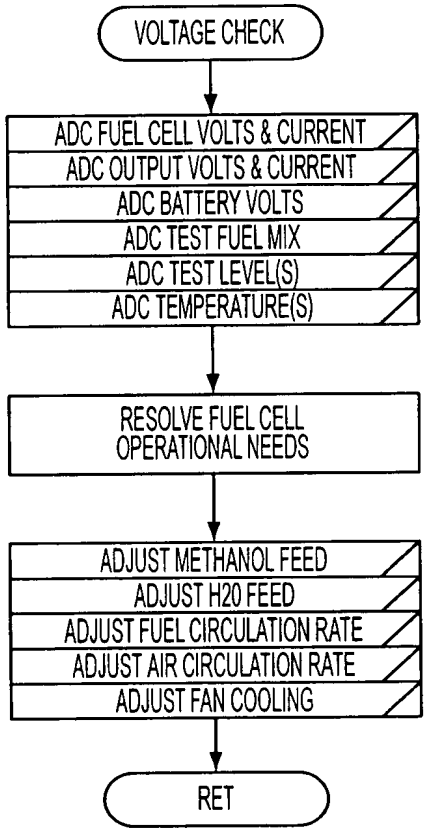
VOLTAGE CHECK
ADC FUEL CELL VOLTS & CURRENT
ADC OUTPUT VOLTS & CURRENT
ADC BATTERY VOLTS
ADC TEST FUEL MIX
ADC TEST LEVEL(S)
ADC TEMPERATURE(S)
RESOLVE FUEL CELL OPERATIONAL NEEDS
ADJUST METHANOL FEED
ADJUST H20 FEED
ADJUST FUEL CIRCULATION RATE
ADJUST AIR CIRCULATION RATE
ADJUST FAN COOLING
RET

FIG. 8D

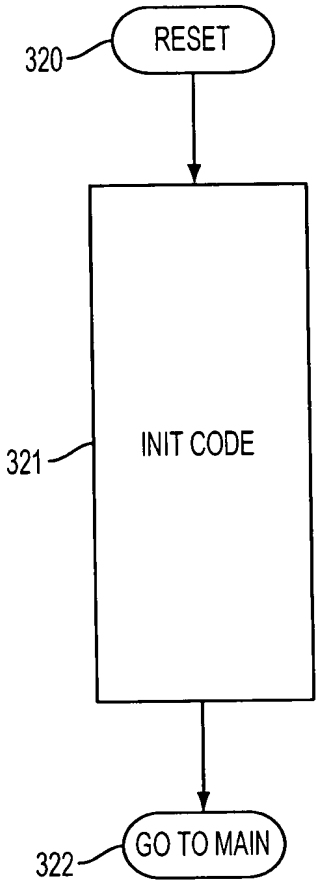

FIG. 9

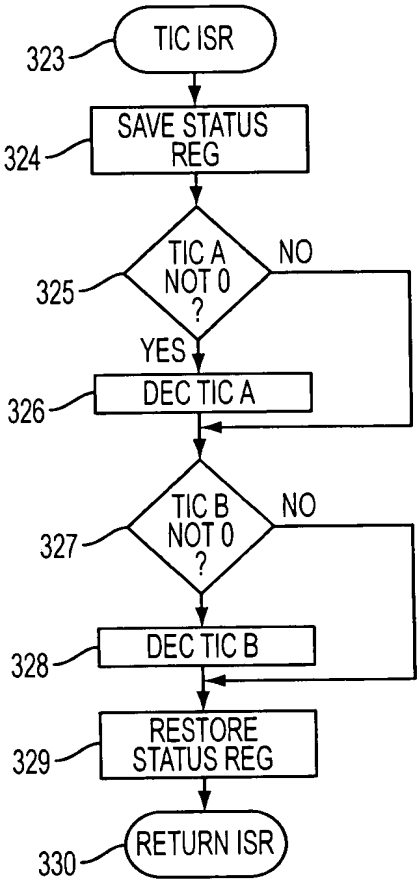

FIG. 10

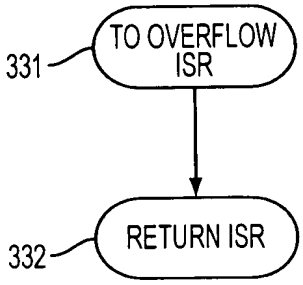

FIG. 11

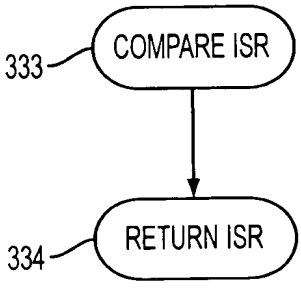

FIG. 12

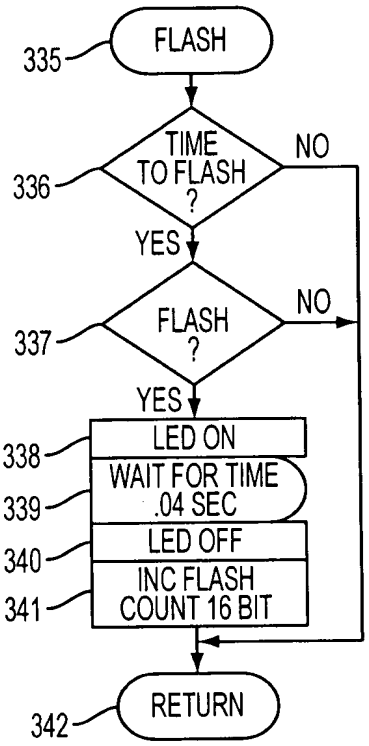

FIG. 13

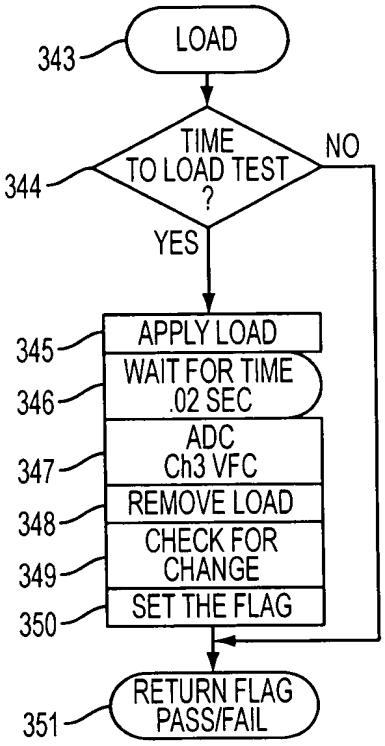

FIG. 14

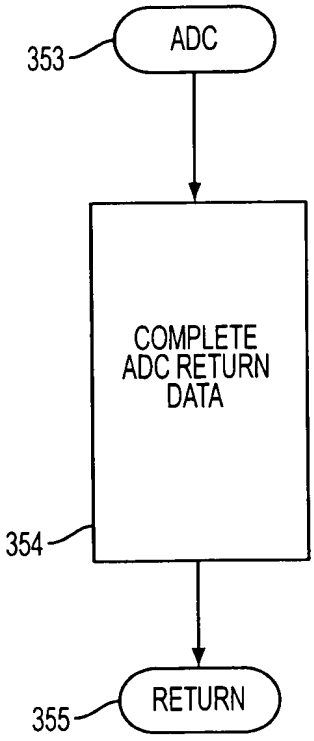

FIG. 15

FIG. 16

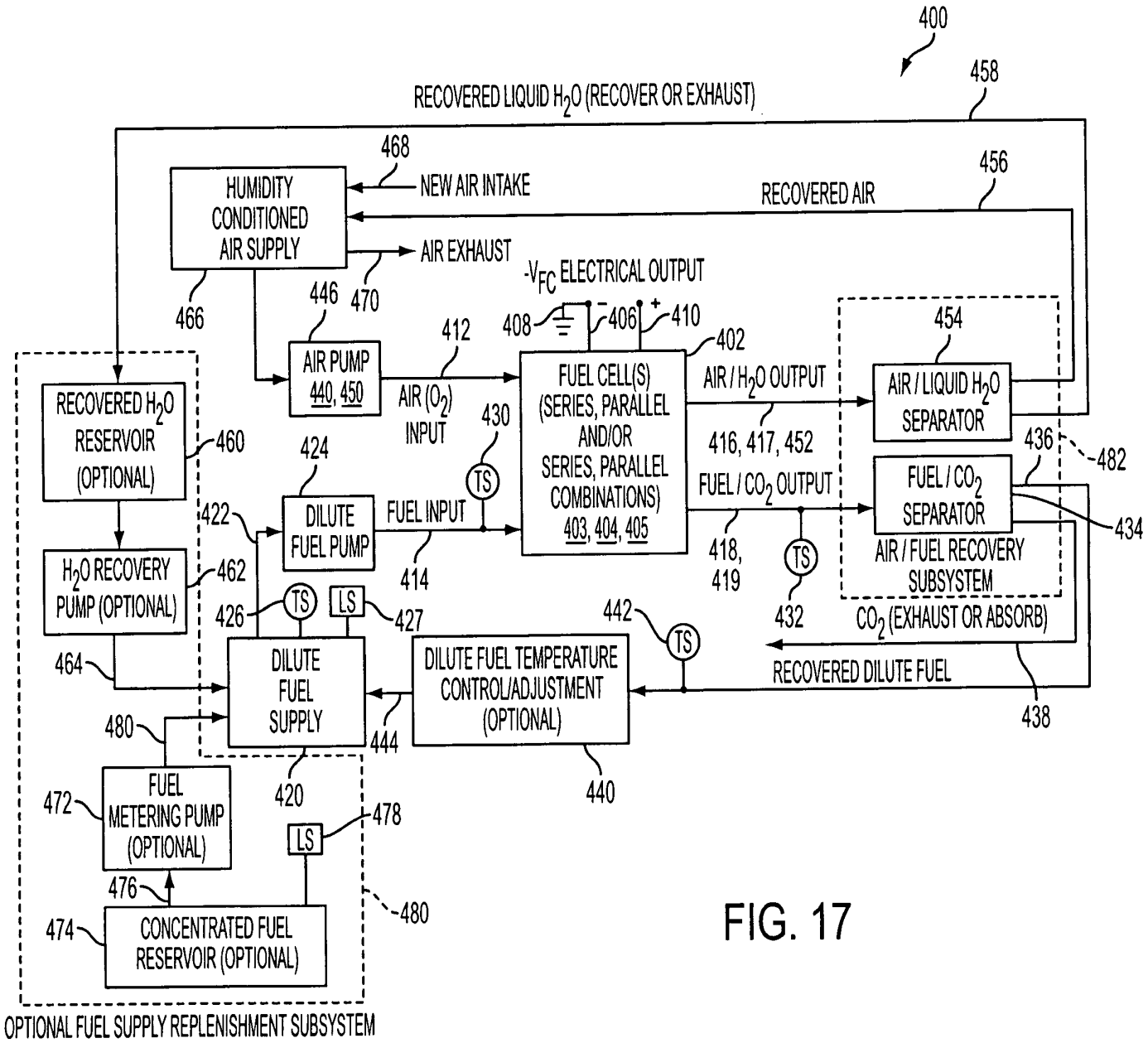
400
RECOVERED LIQUID H_2O (RECOVER OR EXHAUST)
458
468
HUMIDITY CONDITIONED AIR SUPPLY
NEW AIR INTAKE
RECOVERED AIR
456
AIR EXHAUST
$-V_{FC}$ ELECTRICAL OUTPUT
466
446
470
408
406
410
412
402
454
AIR PUMP 440, 450
AIR (O_2) INPUT
FUEL CELL(S) (SERIES, PARALLEL AND/OR SERIES, PARALLEL COMBINATIONS) 403, 404, 405
AIR / H_2O OUTPUT
AIR / LIQUID H_2O SEPARATOR
RECOVERED H_2O RESERVOIR (OPTIONAL)
460
424
430
TS
416, 417, 452
FUEL / CO_2 OUTPUT
436
482
422
DILUTE FUEL PUMP
FUEL INPUT
FUEL / CO_2 SEPARATOR
434
H_2O RECOVERY PUMP (OPTIONAL)
462
414
418, 419
AIR / FUEL RECOVERY SUBSYSTEM
426
LS
427
442
432
CO_2 (EXHAUST OR ABSORB)
464
DILUTE FUEL SUPPLY
DILUTE FUEL TEMPERATURE CONTROL/ADJUSTMENT (OPTIONAL)
RECOVERED DILUTE FUEL
438
480
444
420
440
472
FUEL METERING PUMP (OPTIONAL)
478
476
480
474
CONCENTRATED FUEL RESERVOIR (OPTIONAL)
OPTIONAL FUEL SUPPLY REPLENISHMENT SUBSYSTEM

FIG. 17

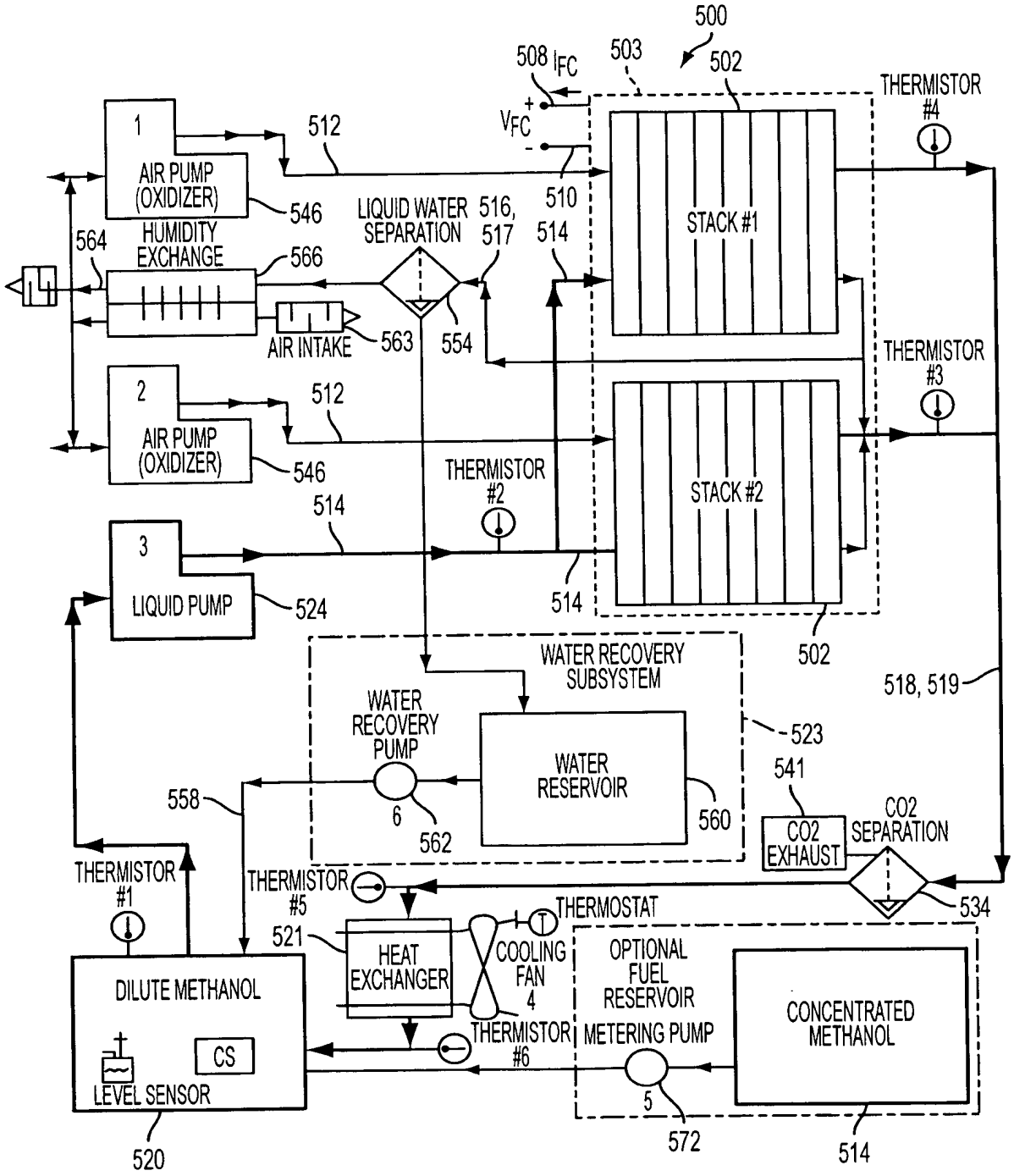
500
508 IFC
503
502
VFC
+
-
THERMISTOR #4
1
AIR PUMP (OXIDIZER)
546
512
510
LIQUID WATER SEPARATION
516, 517
514
STACK #1
564
HUMIDITY EXCHANGE
566
AIR INTAKE
563
554
THERMISTOR #3
2
AIR PUMP (OXIDIZER)
546
512
THERMISTOR #2
STACK #2
514
3
LIQUID PUMP
524
514
502
WATER RECOVERY SUBSYSTEM
518, 519
WATER RECOVERY PUMP
6
562
WATER RESERVOIR
560
523
541
CO2 EXHAUST
CO2 SEPARATION
534
558
THERMISTOR #1
THERMISTOR #5
THERMOSTAT
521
HEAT EXCHANGER
COOLING FAN 4
OPTIONAL FUEL RESERVOIR
DILUTE METHANOL
CS
LEVEL SENSOR
THERMISTOR #6
METERING PUMP
5
572
CONCENTRATED METHANOL
520
514

FIG. 18

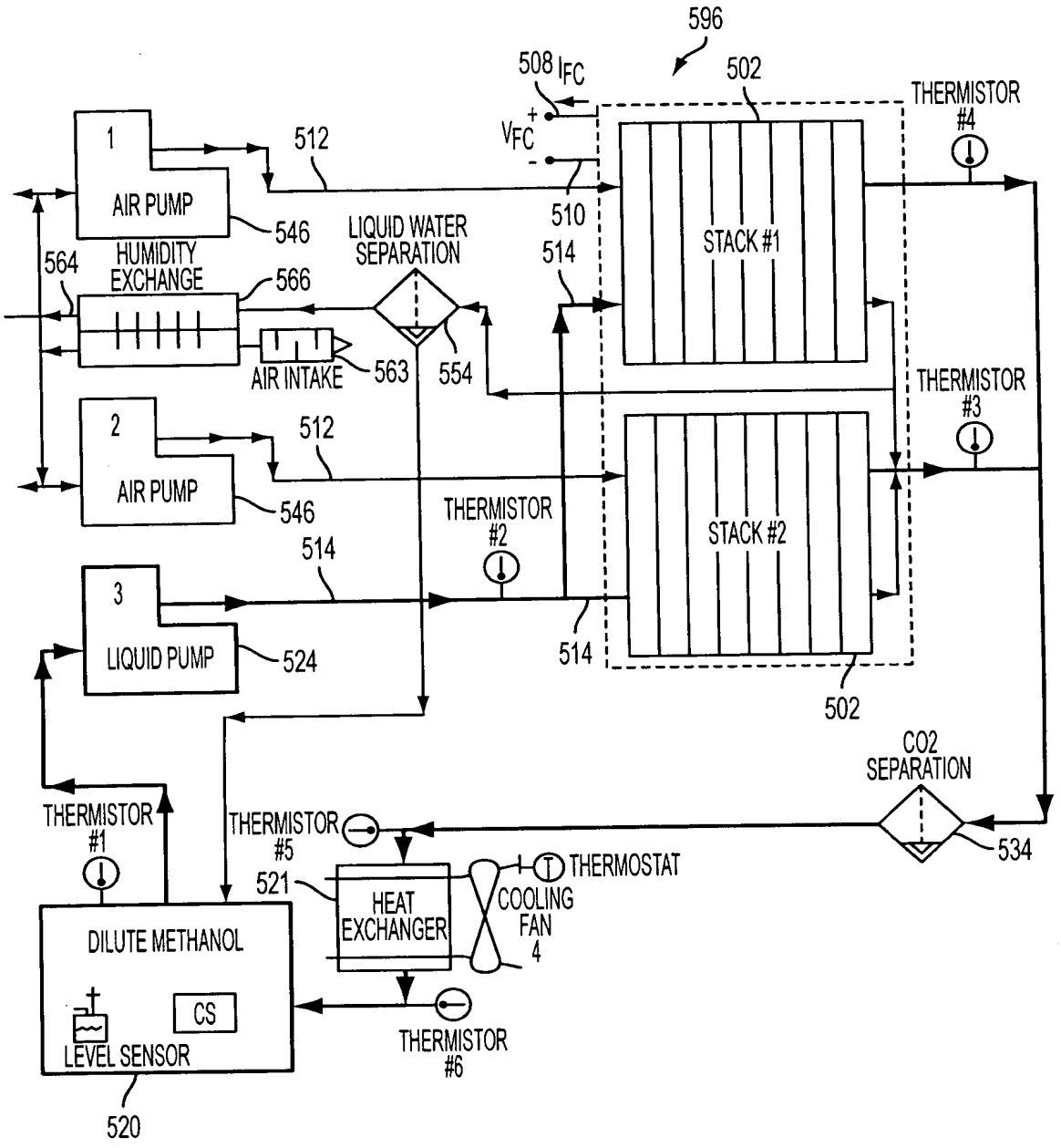
596
508 I_{FC}
502
THERMISTOR #4
V_{FC}
+
-
1
AIR PUMP
546
512
510
STACK #1
LIQUID WATER SEPARATION
514
564
HUMIDITY EXCHANGE
566
AIR INTAKE
563
554
THERMISTOR #3
2
AIR PUMP
546
512
STACK #2
THERMISTOR #2
514
3
LIQUID PUMP
524
514
502
CO2 SEPARATION
534
THERMISTOR #1
THERMISTOR #5
521
HEAT EXCHANGER
THERMOSTAT
COOLING FAN 4
DILUTE METHANOL
CS
LEVEL SENSOR
THERMISTOR #6
520

FIG. 19

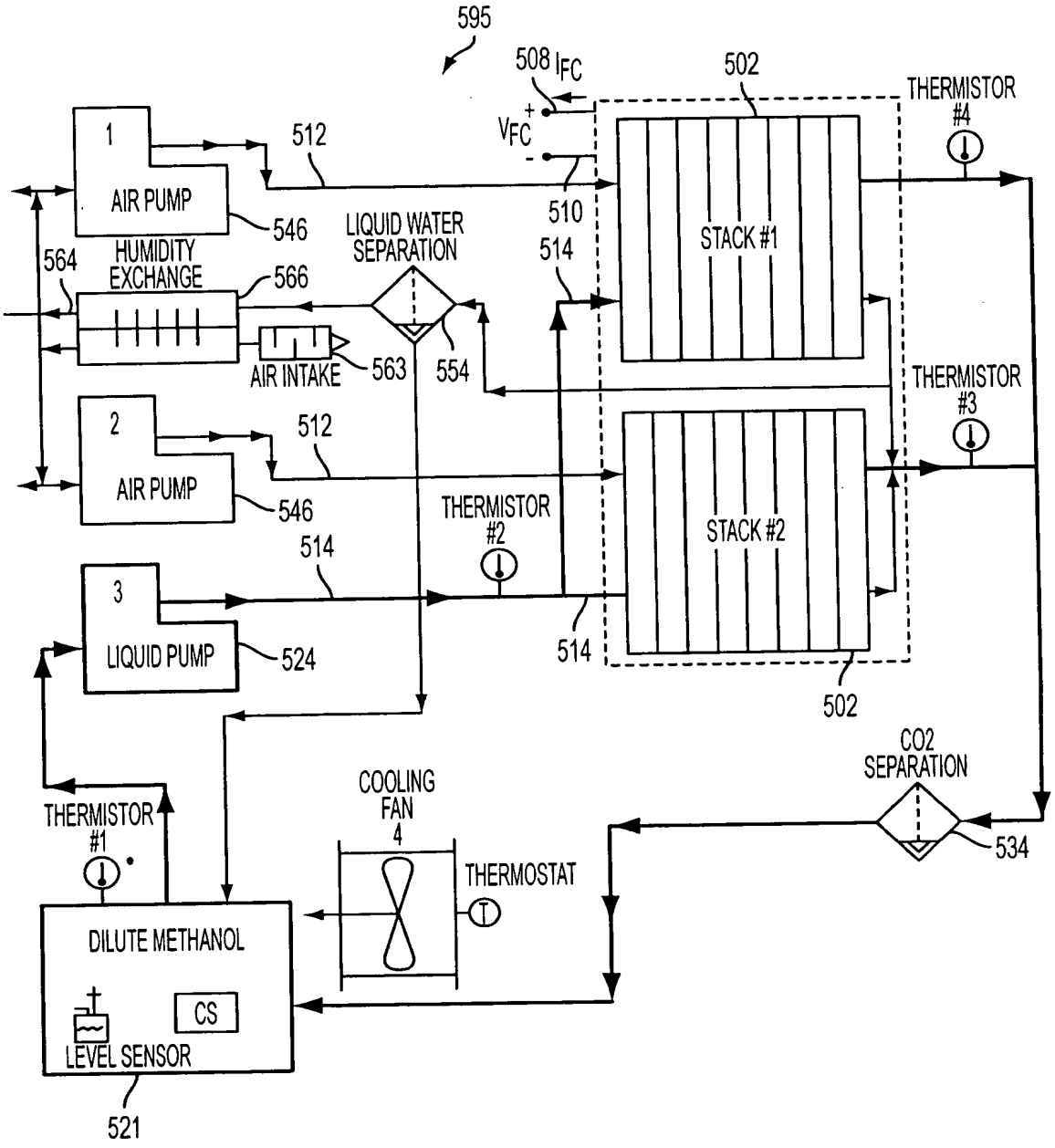
595
508 I_{FC}
502
THERMISTOR #4
V_{FC} + -
1
AIR PUMP
546
512
510
LIQUID WATER SEPARATION
514
STACK #1
564
HUMIDITY EXCHANGE
566
AIR INTAKE
563
554
THERMISTOR #3
2
AIR PUMP
546
512
THERMISTOR #2
STACK #2
514
3
LIQUID PUMP
524
514
502
CO2 SEPARATION
534
COOLING FAN 4
THERMISTOR #1
THERMOSTAT
DILUTE METHANOL
CS
LEVEL SENSOR
521

FIG. 20

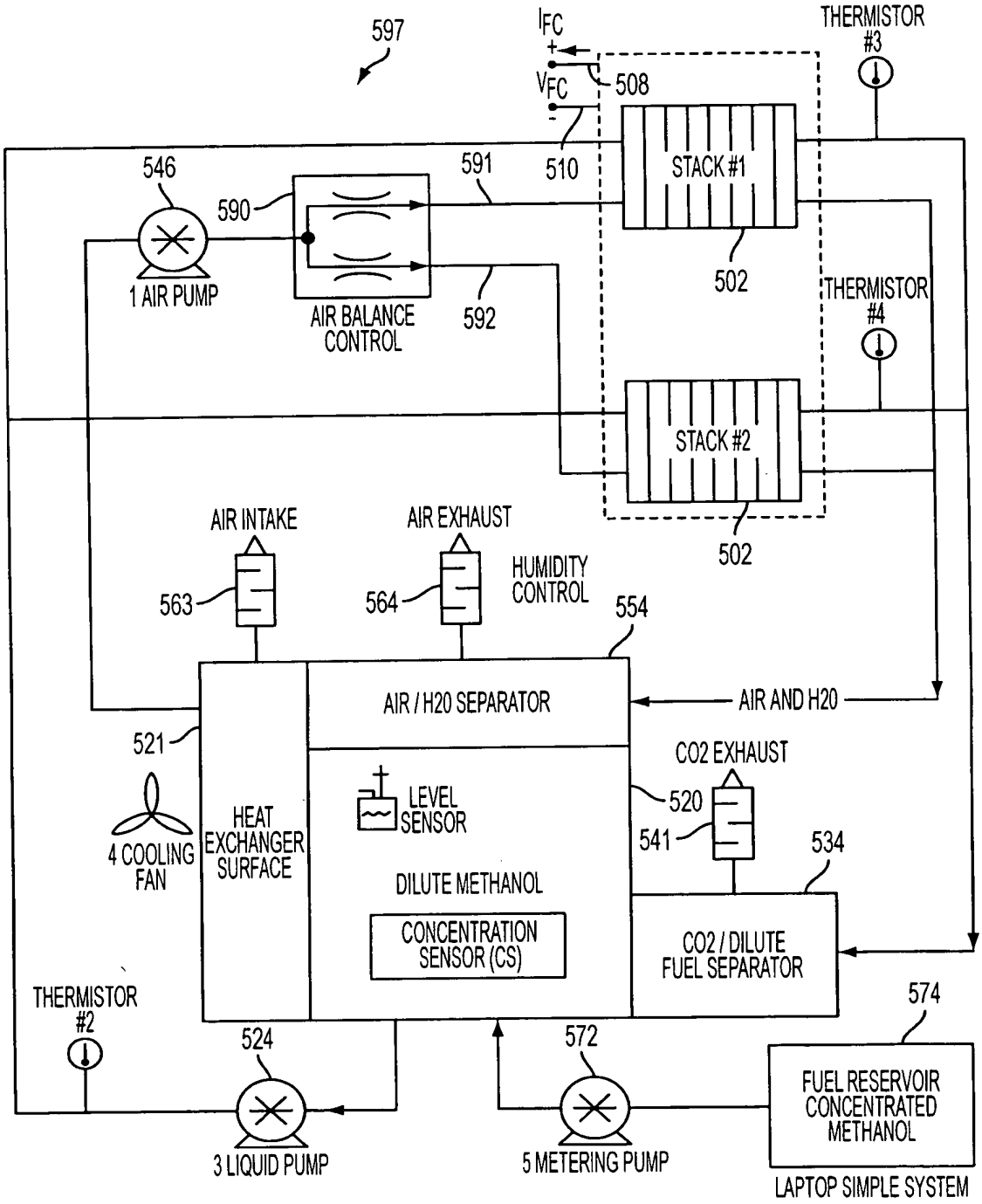
597
IFC
+
VFC
-
508
510
THERMISTOR #3
546
590
591
STACK #1
502
1 AIR PUMP
AIR BALANCE CONTROL
592
THERMISTOR #4
STACK #2
502
AIR INTAKE
AIR EXHAUST
563
564
HUMIDITY CONTROL
554
AIR / H20 SEPARATOR
AIR AND H20
521
CO2 EXHAUST
520
541
534
4 COOLING FAN
HEAT EXCHANGER SURFACE
LEVEL SENSOR
DILUTE METHANOL
CONCENTRATION SENSOR (CS)
CO2 / DILUTE FUEL SEPARATOR
THERMISTOR #2
524
572
574
FUEL RESERVOIR CONCENTRATED METHANOL
3 LIQUID PUMP
5 METERING PUMP
LAPTOP SIMPLE SYSTEM

FIG. 21

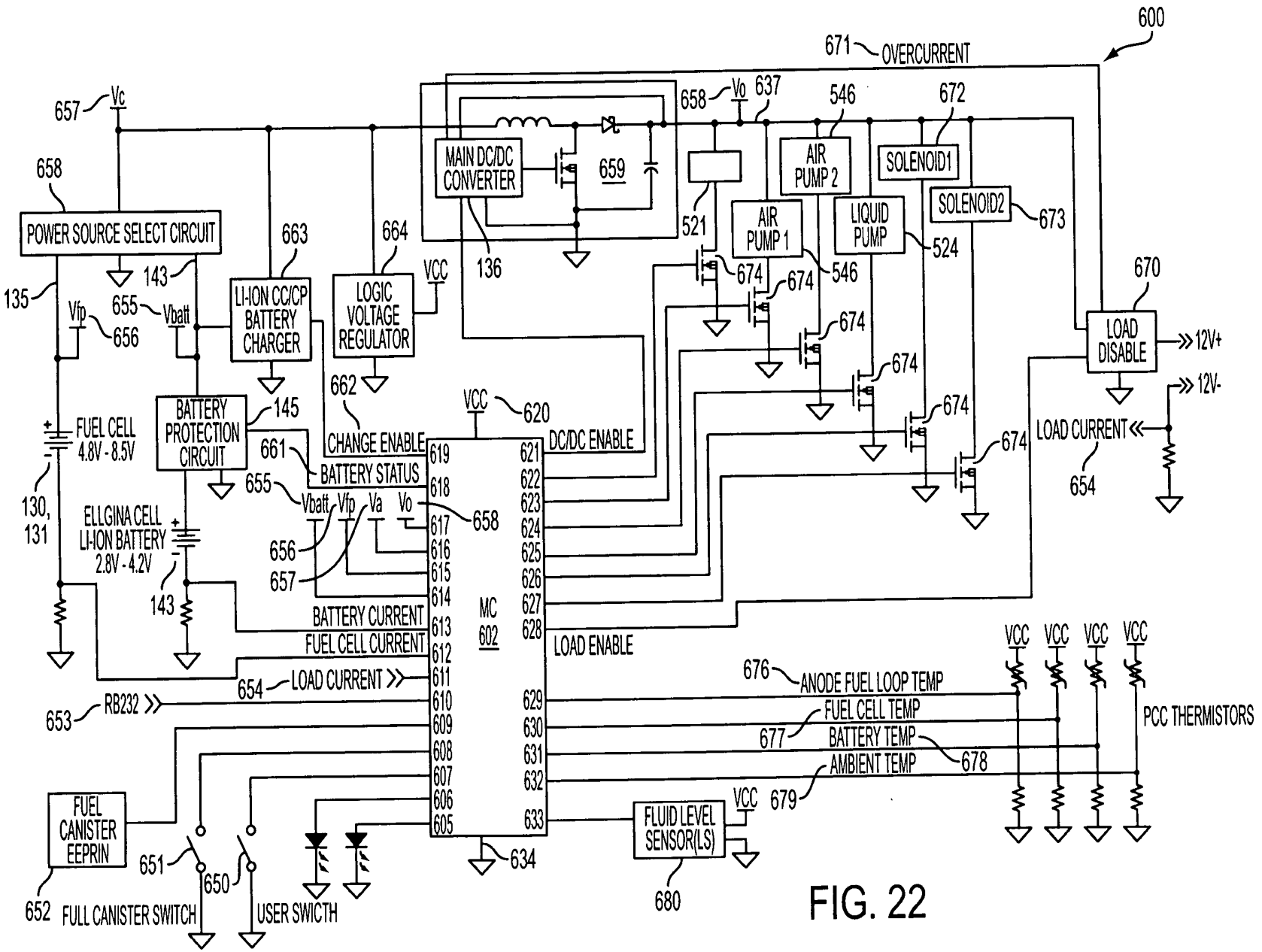
600
671
OVERCURRENT
657
Vc
658
Vo
637
546
672
MAIN DC/DC CONVERTER
659
AIR PUMP 2
SOLENOID1
SOLENOID2
673
521
AIR PUMP 1
LIQUID PUMP
524
674
546
670
LOAD DISABLE
12V+
12V-
POWER SOURCE SELECT CIRCUIT
663
664
VCC
136
143
135
655
Vbatt
Vfp
656
LI-ION CC/CP BATTERY CHARGER
LOGIC VOLTAGE REGULATOR
662
CHANGE ENABLE
620
DC/DC ENABLE
145
BATTERY PROTECTION CIRCUIT
661
BATTERY STATUS
FUEL CELL 4.8V - 8.5V
130, 131
ELLGINA CELL LI-ION BATTERY 2.8V - 4.2V
Va
MC 602
LOAD CURRENT
654
BATTERY CURRENT
FUEL CELL CURRENT
LOAD ENABLE
676
ANODE FUEL LOOP TEMP
FUEL CELL TEMP
677
BATTERY TEMP
678
AMBIENT TEMP
679
PCC THERMISTORS
653
RB232
FUEL CANISTER EEPRIN
652
651
650
FULL CANISTER SWITCH
USER SWICTH
634
FLUID LEVEL SENSOR(LS)
680

FIG. 22

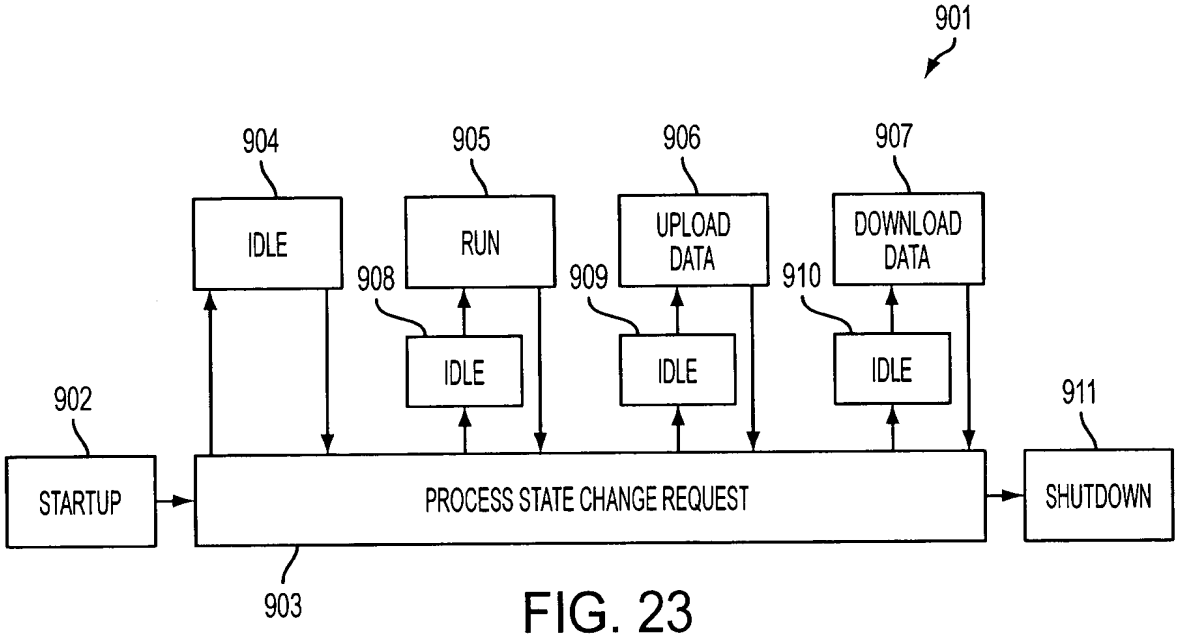
901
904
905
906
907
IDLE
RUN
UPLOAD DATA
DOWNLOAD DATA
908
909
910
IDLE
IDLE
IDLE
902
911
STARTUP
PROCESS STATE CHANGE REQUEST
SHUTDOWN
903

FIG. 23

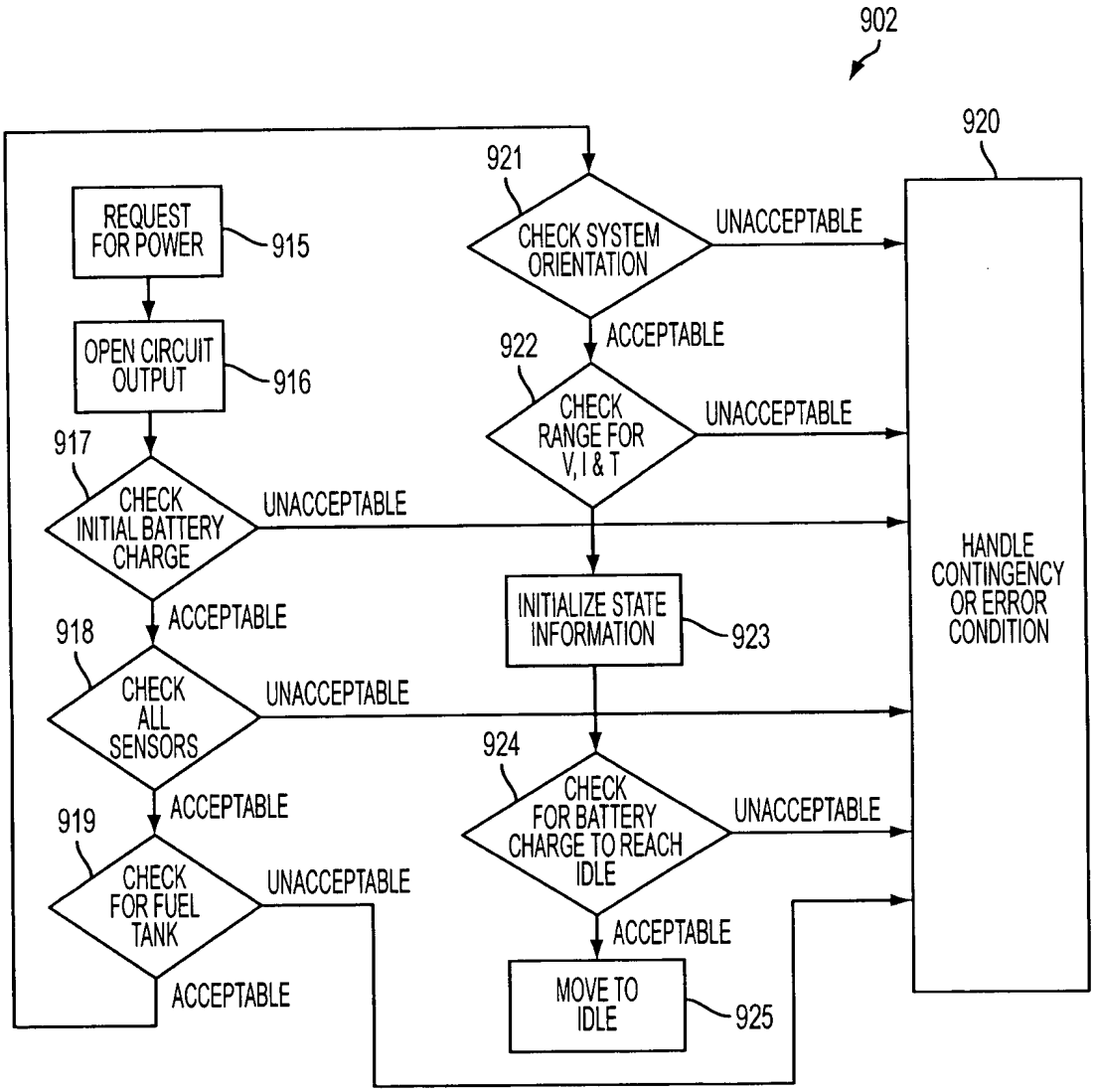
902
920
921
REQUEST FOR POWER
915
CHECK SYSTEM ORIENTATION
UNACCEPTABLE
OPEN CIRCUIT OUTPUT
916
ACCEPTABLE
922
CHECK RANGE FOR V, I & T
UNACCEPTABLE
917
CHECK INITIAL BATTERY CHARGE
UNACCEPTABLE
HANDLE CONTINGENCY OR ERROR CONDITION
ACCEPTABLE
INITIALIZE STATE INFORMATION
923
918
CHECK ALL SENSORS
UNACCEPTABLE
924
ACCEPTABLE
CHECK FOR BATTERY CHARGE TO REACH IDLE
UNACCEPTABLE
919
CHECK FOR FUEL TANK
UNACCEPTABLE
ACCEPTABLE
MOVE TO IDLE
925

FIG. 24

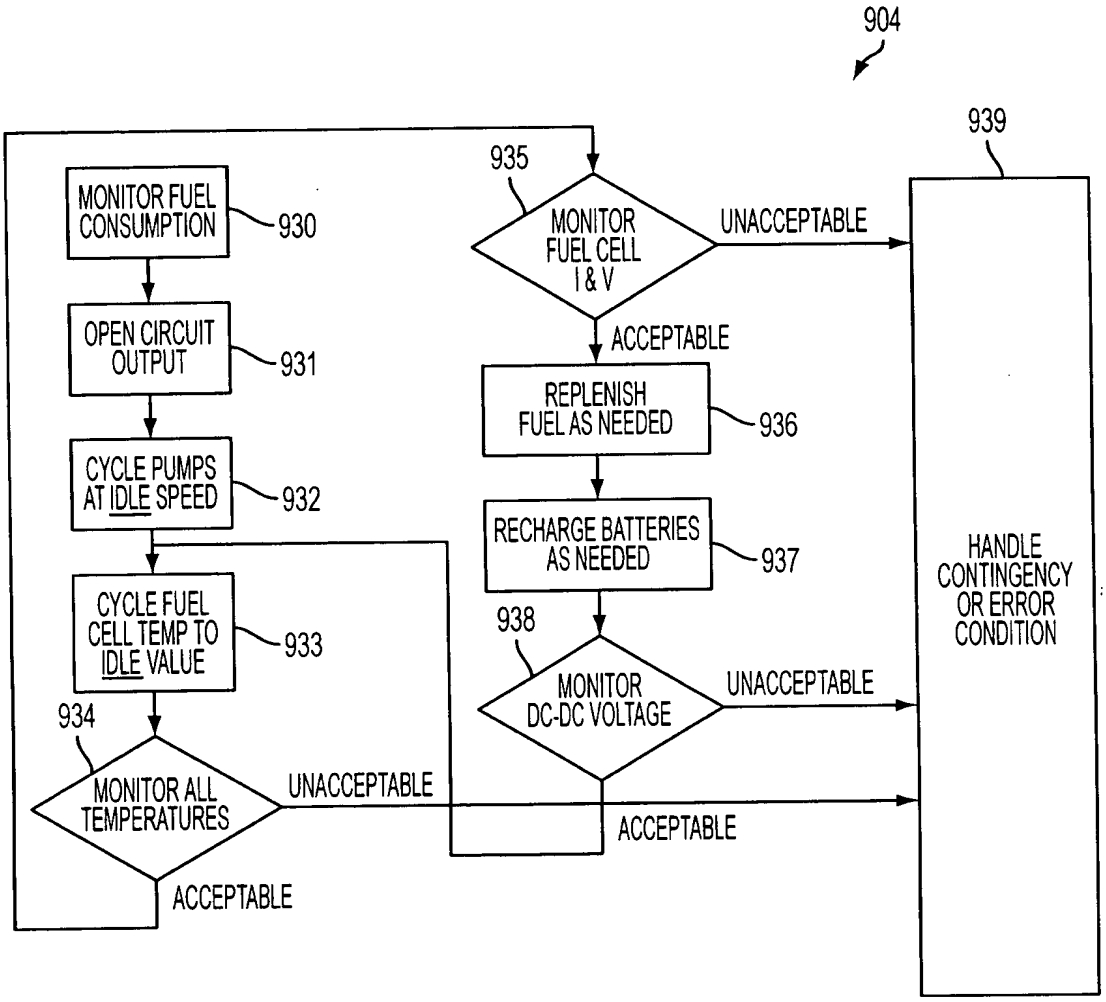
904
939
935
MONITOR FUEL CONSUMPTION
930
MONITOR FUEL CELL I & V
UNACCEPTABLE
OPEN CIRCUIT OUTPUT
931
ACCEPTABLE
REPLENISH FUEL AS NEEDED
936
CYCLE PUMPS AT IDLE SPEED
932
RECHARGE BATTERIES AS NEEDED
937
HANDLE CONTINGENCY OR ERROR CONDITION
CYCLE FUEL CELL TEMP TO IDLE VALUE
933
938
MONITOR DC-DC VOLTAGE
UNACCEPTABLE
934
MONITOR ALL TEMPERATURES
UNACCEPTABLE
ACCEPTABLE
ACCEPTABLE

FIG. 25

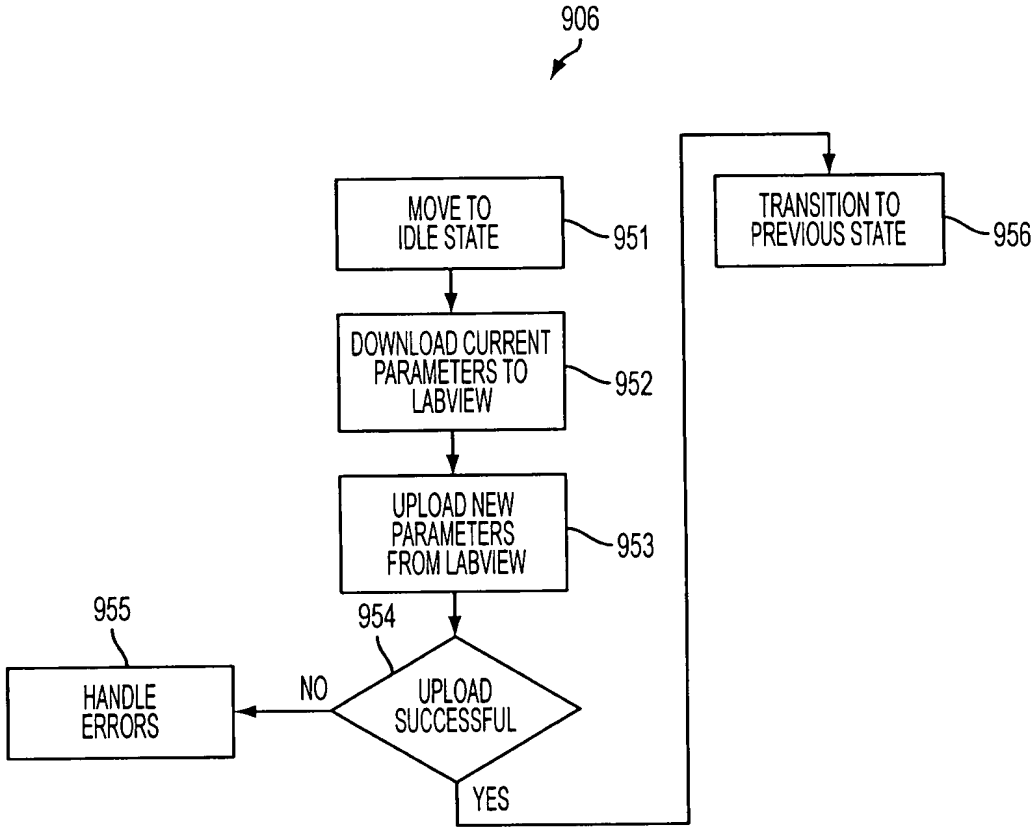
906
MOVE TO IDLE STATE
951
DOWNLOAD CURRENT PARAMETERS TO LABVIEW
952
UPLOAD NEW PARAMETERS FROM LABVIEW
953
954
UPLOAD SUCCESSFUL
NO
HANDLE ERRORS
955
YES
TRANSITION TO PREVIOUS STATE
956

FIG. 26

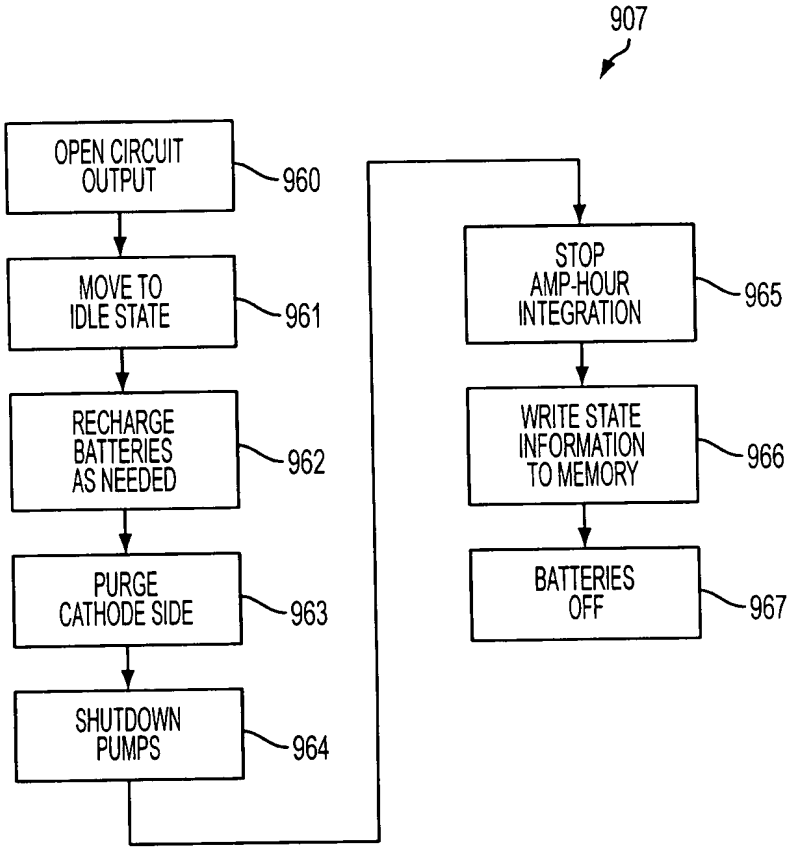
907
OPEN CIRCUIT OUTPUT
960
MOVE TO IDLE STATE
961
RECHARGE BATTERIES AS NEEDED
962
PURGE CATHODE SIDE
963
SHUTDOWN PUMPS
964
STOP AMP-HOUR INTEGRATION
965
WRITE STATE INFORMATION TO MEMORY
966
BATTERIES OFF
967

FIG. 27

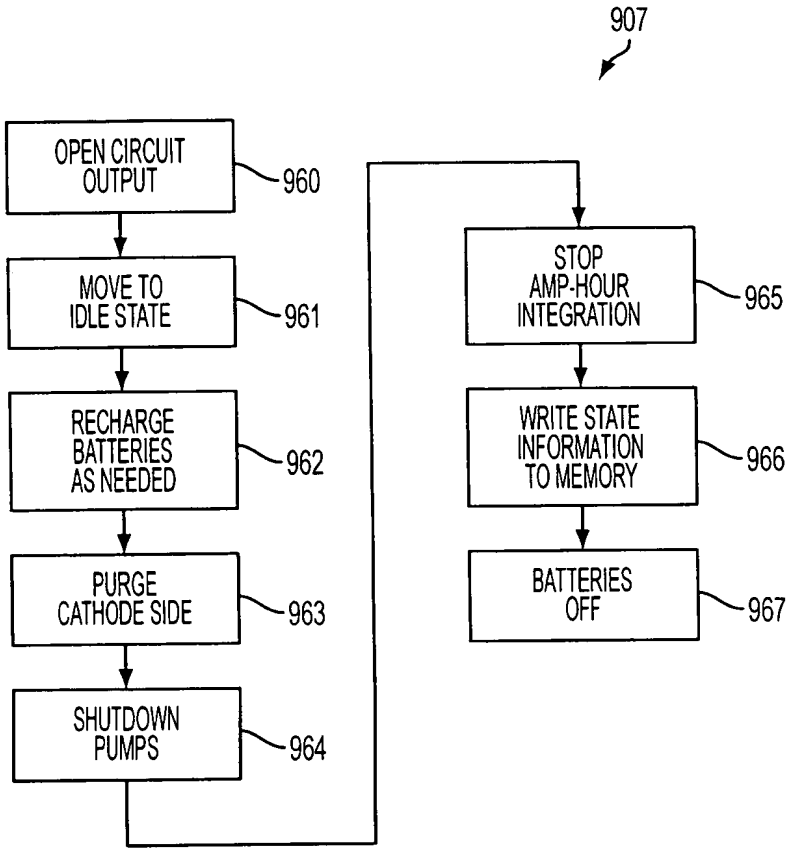
907
OPEN CIRCUIT OUTPUT
960
MOVE TO IDLE STATE
961
RECHARGE BATTERIES AS NEEDED
962
PURGE CATHODE SIDE
963
SHUTDOWN PUMPS
964
STOP AMP-HOUR INTEGRATION
965
WRITE STATE INFORMATION TO MEMORY
966
BATTERIES OFF
967

FIG. 28

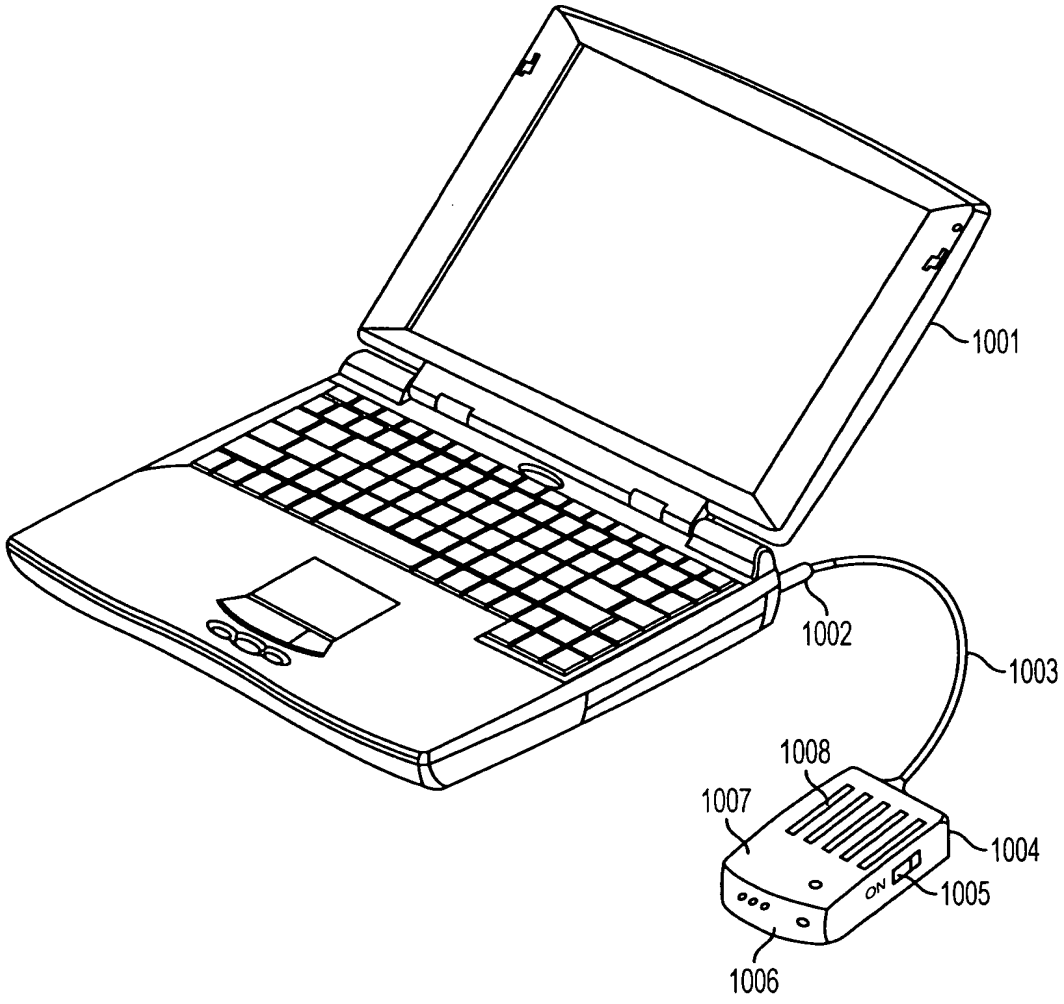

FIG. 29